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WAVETEK SAN DIEGO, INC.

9045 Balboa Ave., San Diego, CA 92123

USER GUIDE

MODEL 2000 SPG Series
SYSTEM PULSE GENERATOR

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SAFETY FIRST

Protect yourself. Follow these precautions.

- Don't touch the outputs of the instrument or any exposed test wiring carrying the output signals. This instrument can generate hazardous voltages and currents.
- Don't bypass the power cord's ground lead with two-wire extension cords or plug adaptors.
- Don't disconnect the green and yellow safety-earth-ground wire that connects the ground lug of the power receptacle to the chassis ground terminal (marked with ⏚ or ⚠).
- Don't hold your eyes extremely close to an rf output for a long time. The normally nonhazardous low-power rf energy generated by the instrument could possibly cause eye injury.
- Don't plug in the power cord until directed to by the installation instructions.
- Don't repair the instrument unless you are a qualified electronics technician and know how to work with hazardous voltages.
- Pay attention to the **WARNING** statements. They point out situations that can cause injury or death.
- Pay attention to the CAUTION statements. They point out situations that can cause equipment damage.

EH ELECTRONICS
SYSTEM PULSE GENERATOR

SPG2000 Series User Guide

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MODEL SPG2000

SECTION 1

SYSTEM OVERVIEW

SECTION 1 SYSTEM OVERVIEW

This manual applies to the Series 2000 System Pulse Generators (SPG) which include Models 2005, 2010, and future additions. Unless specified, information herein refers to all three models.

1.1 SPG FEATURES

The SPG is a fully programmable, fast rise time, high performance pulse generator with 200 MHz operation and sub nanosecond (Model 2005) rise times. It is intended for automatic test equipment applications. Some typical uses are:

- fast discrete device testing
- integrated circuit testing
- module and subassembly testing
- subsystem testing

Although the SPG is designed for fully automatic operation from either IEEE-488 or RS-232-C interfaces, there are optional front panel display and controls available which give the operator full manual control of pulse parameters.

A CRT display is available which shows a graphic representation of the output waveforms as well as the values of all pulse parameters and modes. Four output channels per unit are available.

Forty setups are stored in the SPG's internal memory registers, the first five of which are non-volatile. A setup is defined as the set of all the pulse parameter values for four channels.

Figure 1-1 shows a picture of an SPG.

1.2 BLOCK DIAGRAM

Figure 1-2 is a block diagram of an SPG. It consists of computation and control, graphic display, clock, power supply and channel boards. The channel boards are paired with an output driver module at the factory and are calibrated as a matched set.

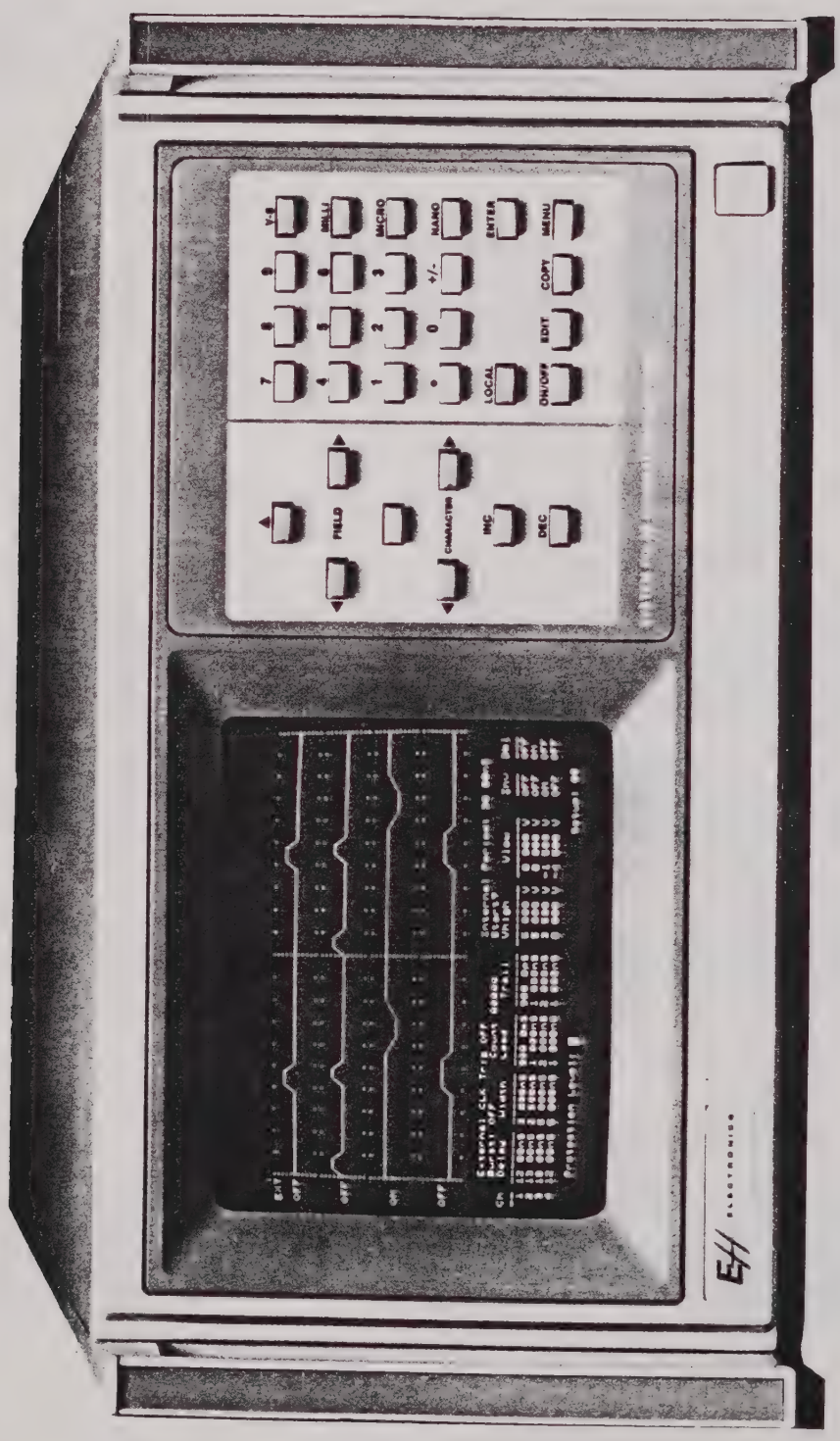

MILLI
MICRO
NANO
ENTER
COPY
MENU
EDIT
LOCAL
ON/OFF
FIELD
CHARACTER
INC
DEC

Figure 1-1

SPG 2000 SERIES BLOCK DIAGRAM
INTERNAL BUSS

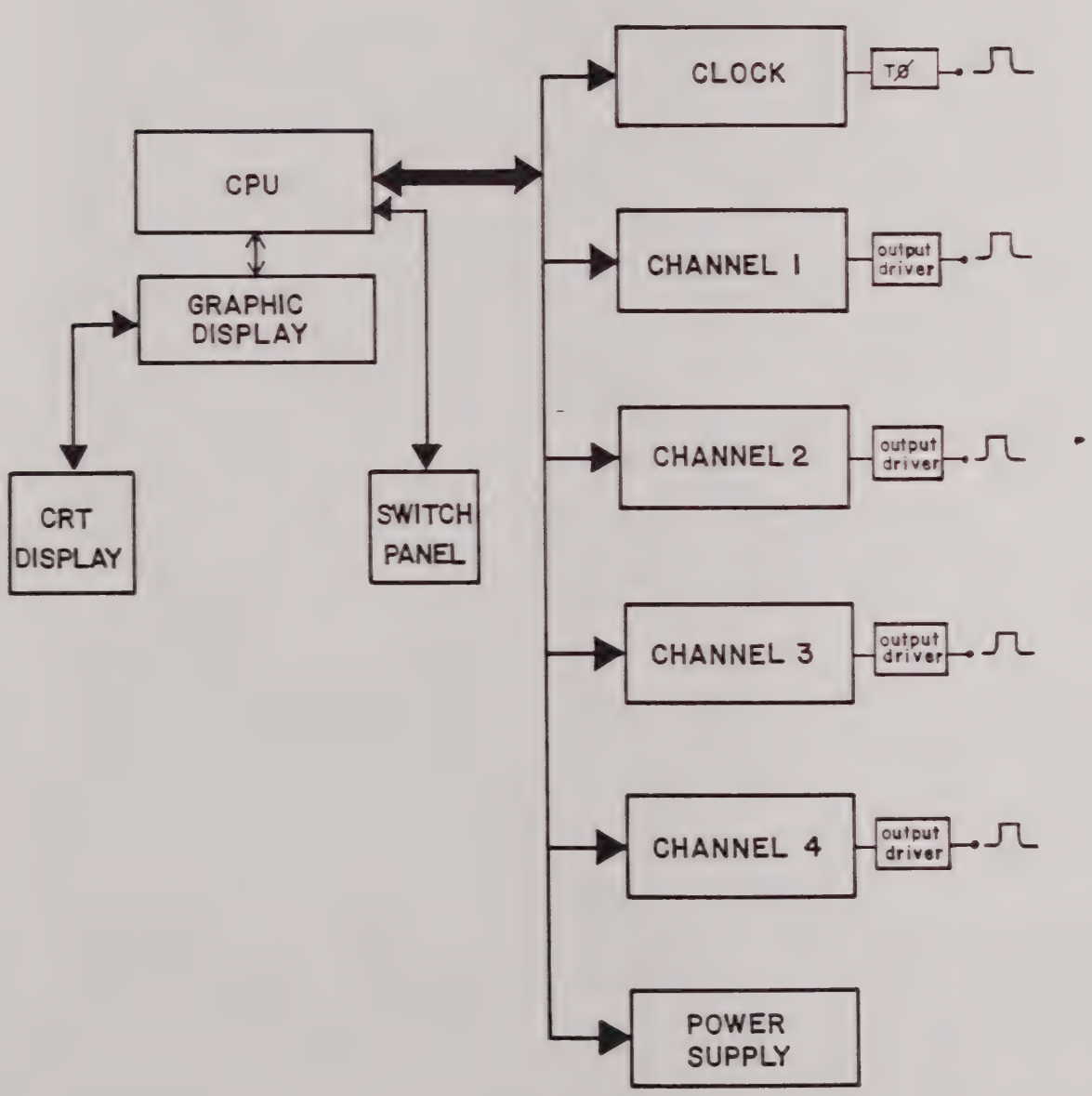


Figure 1-2

MODEL SPG2000

SECTION 2

INSTALLATION

SECTION 2 INSTALLATION

2.1 UNPACKING THE SPG

Inspect the shipping container for damage. If the container or cushioning material is damaged, it should be kept until the contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically.

Verify the contents of your shipment against the packing slip. Report any shortages to your EH Electronics' sales representative or directly to EH Electronics.

If there is no apparent damage, place the instrument along with any accessories on a table or bench top and inspect for:

- loose hardware
- damaged connectors on rear panel
- push buttons and switches which do not operate smoothly

2.2 DAMAGED EQUIPMENT

Under normal terms and conditions of sale, when a carrier has accepted the shipment at the EH factory, the goods become the buyer's property. The buyer is therefore responsible for any claims of loss or damage to those goods. Any damage found during unpacking and inspection must be reported to the carrier.

2.3 VOLTAGE SELECTION

The SPG can operate with 100, 120, 220 or 240 V AC (+10%), 50 to 60 Hz. It is equipped with an external voltage selecting and fused connector.

To select the voltage (Refer to Figure 2-1):

1. Remove plug if present.

2. Slide cover door of the connector to the left.

3. Pull FUSE PULL tab out and to the left. The fuse will be pushed out and should be removed.

4. Remove the PC board.

5. Select operating voltage by orienting the PC board such that the value of the desired voltage is positioned on the top left of the board. The voltage values printed on the PC board are 100, 120, 220 and 240.

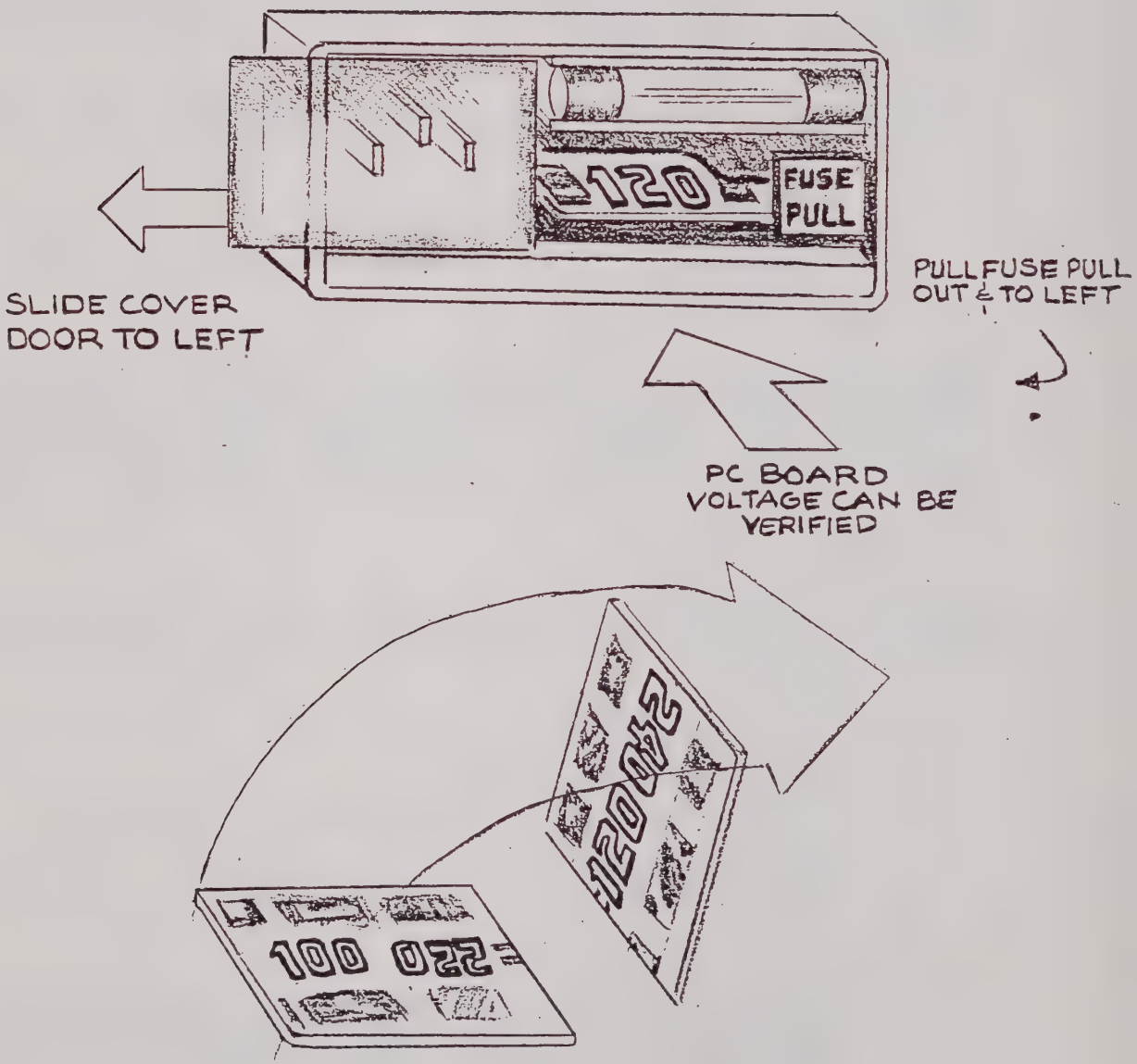

120
FUSE
PULL
SLIDE COVER
DOOR TO LEFT
PULL FUSE PULL
OUT & TO LEFT
PC BOARD
VOLTAGE CAN BE
VERIFIED
100 220
220 120

FIGURE 2-1

6. Push board firmly into the slot.

7. Push FUSE PULL tab to the right (back to normal position). The value of the operating voltage can now be seen and verified.

8. Insert proper fuse into holders. See chart below.

Voltage	SB Fuse (amp)
100	5
120	5
220	2.5
240	2.5

9. Slide cover door to the right.

2.4 EXTENSION CORD USAGE

In accordance with international safety standards, the unit is equipped with a three-wire power cable. When connected to an appropriate AC receptacle, this cable grounds the instrument cabinet. The protective action of the plug must not be negated by use of an extention cord without a protective conductor.

2.5 RACK MOUNTING

When rack mounting the unit with other equipment, be sure that warm air exhaust from another instrument is not being drawn into the SPG's rear panel air cooling intake. The unit should be supported along its length by either rack rails or rack slides. Option 04 may be ordered from EH Electronics to provide rack slides. Do not mount the unit by the front panel alone.

2.6 SIGNAL CONNECTIONS AND TERMINATIONS

The SPG output contains frequency components greater than 1 GHz on the fastest rise and fall time ranges, therefore it is important to provide proper signal terminations. If any of the connectors, cables or attenuators used do not have flat responses beyond 1 GHz, degradation of pulse rise time will result.

The output of the SPG is backmatched to minimize pulse distortion due to mismatched loads. The SPG should be terminated in a 50 OHM load at all times. Use only high quality 50 OHM terminations.

2.7 STORED EQUIPMENT

The instrument can be stored or shipped at temperatures between -20 degC and +70 degC. It should be protected against conditions which cause condensation within the instrument.

CAUTION: Because of the shelf life of electrolytic capacitors, a unit placed in storage for six months or more should be connected to a variac and with instrument power on, the line voltage should be gradually increased from 0 V to the specified operating voltage.

2.8 SHIPPING OF EQUIPMENT

It is recommended that you do not reuse original shipping cartons when shipping equipment. The corrugated cardboard cartons and materials used for shipment to you are designed for one time use only. It is further recommended that you use a strong shipping container. A double walled carton made of 350 pound test material is adequate. Contact EH Electronics for assistance in obtaining a proper carton. Wrap instrument in heavy paper or plastic. Use a three to four inch layer of shock absorbing material around all sides of the instrument to provide a firm cushion and prevent movement inside container. Seal container securely and mark it "FRAGILE" to encourage careful handling.

2.9 REAR PANEL CONNECTIONS AND CONTROLS (C2100 VERSION) (Refer to Figure 2-2)

A description of each of the items located on the rear panel shown in Figure 2-2 is given below.

J101	CHNL 1 OUTPUT	Female SMA connector providing the output for Channel 1.
J102	CHNL 2 OUTPUT	Female SMA connector providing the output for Channel 2.
J103	CHNL 3 OUTPUT	Female SMA connector providing the output for Chanel 3.
J104	CHNL 4 OUTPUT	Female SMA connector providing the output for Channel 4.
J105	RS 232	25 pin female "D" connector (DM 258). Provides interface between the SPG and external RS-232-C compatible equipment. See Appendix A.
J106	IEEE 488	24 pin female microribbon (57 series) connector for interface with IEEE-488 compatible equipment. See Appendix B

J107	GATE IN	BNC connector for the input of an external gating signal.
J108	TO OUT	BNC connector for the output of the internal trigger signal.
J109	CLOCK OUT	BNC connector for the output of the internal clock signal. (C2100 ver) Units without connectors J113-J117, J109 is external drive clock input. (See 2.10)
J110	BURST START IN	BNC connector for the input of an external burst start signal.
J111	BURST COMP OUT	BNC conector for the output of the burst complete signal.
J112	AC INPUT	A plug for the line voltage input cable. (Refer to section 2.3 for the procedure to change voltage configuration.)
J113	CLOCK IN	BNC connector for the input of an external drive clock signal.
J114	CHAN 1 IN	BNC connector for the input of an external drive clock signal to drive channel independently of the clock signal from the internal clock board.
J115	CHAN 2 IN	(See J114 above.)
J116	CHAN 3 IN	(See J114 above.)
J117	CHAN 4 IN	(See J114 above.)
F101	(AC FUSE)	Designates the fuse in the voltage selecting and fused connector.
R101	CRT INTENSITY ADJ	Control for adjusting the intensity of the CRT display.

2.10 REAR PANEL CONNECTIONS AND CONTROLS (Without C2100 Clock Board)

Designations are the same as above with the following exceptions.

J109	CLOCK	BNC connector for external drive clock input.
J113-J117		Plugged, not applicable.

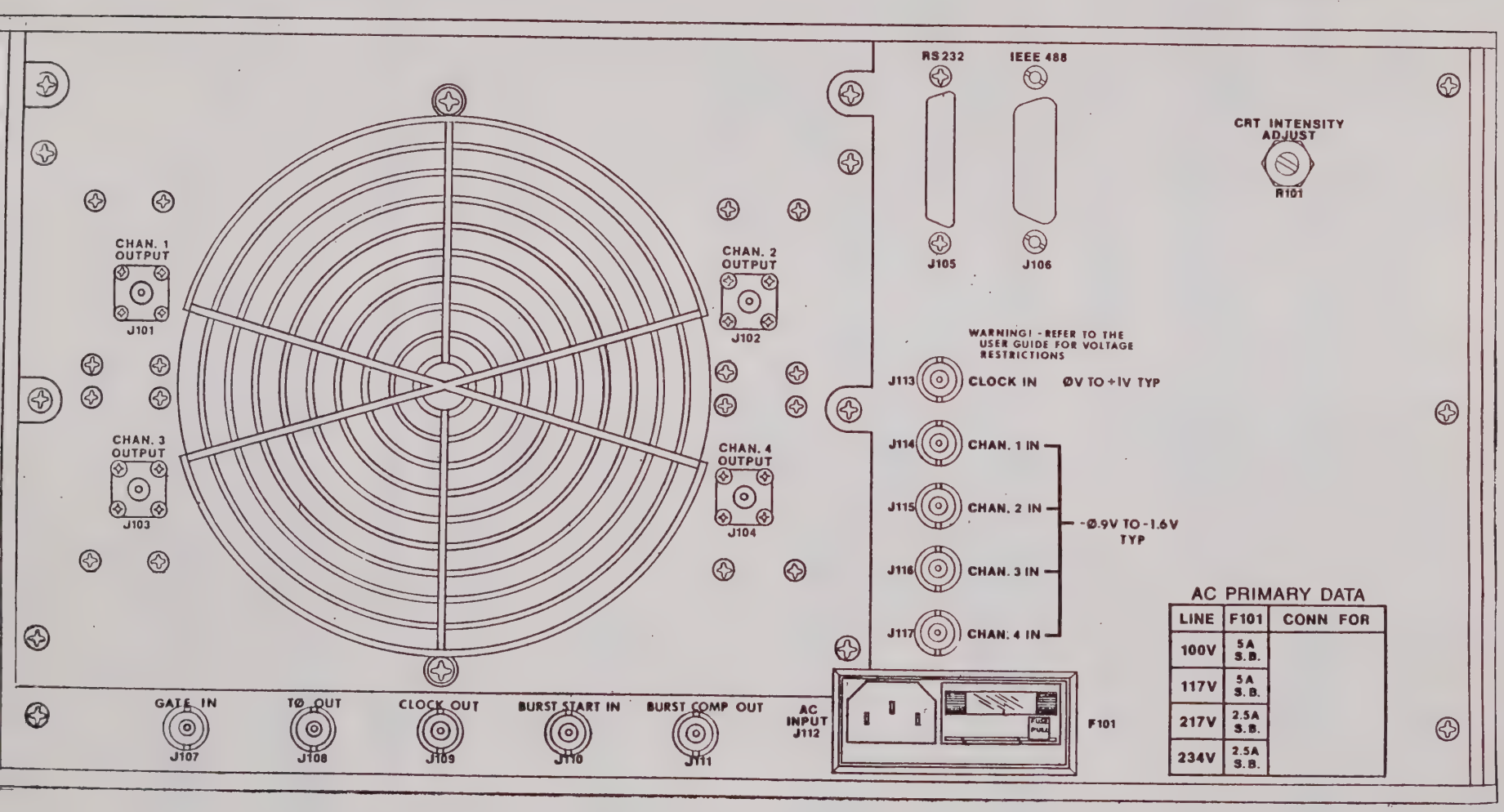

RS232
IEEE 488
CRT INTENSITY ADJUST
R101
J105
J106
CHAN. 1 OUTPUT
J101
CHAN. 2 OUTPUT
J102
CHAN. 3 OUTPUT
J103
CHAN. 4 OUTPUT
J104
WARNING! - REFER TO THE USER GUIDE FOR VOLTAGE RESTRICTIONS
J113 CLOCK IN ØV TO +1V TYP
J114 CHAN. 1 IN
J115 CHAN. 2 IN
J116 CHAN. 3 IN
J117 CHAN. 4 IN
-Ø.9V TO -1.6V TYP
AC PRIMARY DATA
LINE | F101 | CONN FOR
100V | 5A S.B.
117V | 5A S.B.
217V | 2.5A S.B.
234V | 2.5A S.B.
GATE IN J107
TØ OUT J108
CLOCK OUT J109
BURST START IN J110
BURST COMP OUT J111
AC INPUT J112
F101

Figure 2-2

MODEL SPG2000

SECTION 3

OPERATION

SECTION 3 OPERATION

3.1 PULSE PARAMETER DEFINITIONS

The SPG provides full control of the pulse amplitude, delay, period, width and rise and fall times. The pulses can be single or double, normal or inverted, and can be programmed for a specified number of pulses per burst. The following definitions explain what is meant by each parameter.

Period. Pulse period is the time between successive cycles of a pulse train. Refer to Figure 3-1.

Delay. Pulse delay is the time between the leading edge of the trigger output and the 50% amplitude point on the leading edge of the output pulse. Refer to Figure 3-2.

Width. Pulse width is the time between 50% amplitude points on the leading and trailing edges of a pulse. Refer to Figure 3-3. This is valid at the fastest ramp setting only. Other settings of the leading and trailing edges may require an adjustment of the width setting to achieve the desired results.

Rise Time. The rise time is the time from the 10% to 90% amplitude points on the pulse leading edge. Refer to Figure 3-4.

Fall Time. The fall time is the time from the 90% to 10% amplitude points on the pulse trailing edge. Refer to Figure 3-4.

Double Pulse. Pairs of identical pulses within a given period are generated where the first pulse is coincident with the trigger output, and the second pulse begins after the programmed delay. Refer to Figure 3-5.

Burst. A burst of pulses may be programmed to begin on one of several events. When the specified number of pulses have been output, the pulse train stops until the next burst is triggered. Refer to Figure 3-6.

Amplitude. Pulse amplitude is the difference between the high voltage (Vhi) and the low voltage (Vlo) levels. Vhi is always more positive than Vlo. Refer to Figure 3-7.

3.2 POWER-ON STATE

The state in which the SPG comes up after application of power is determined by the values stored in EEPROM. It is therefore up to the user to specify the desired state by saving the appropriate values to EEPROM. This is accomplished either through the Menu for manual operation, or through a series of commands over one of the remote interfaces. The following events occur during the power-on initialization:

1. A System Test is executed.
2. Setups 0 through 4 are loaded from EEPROM.

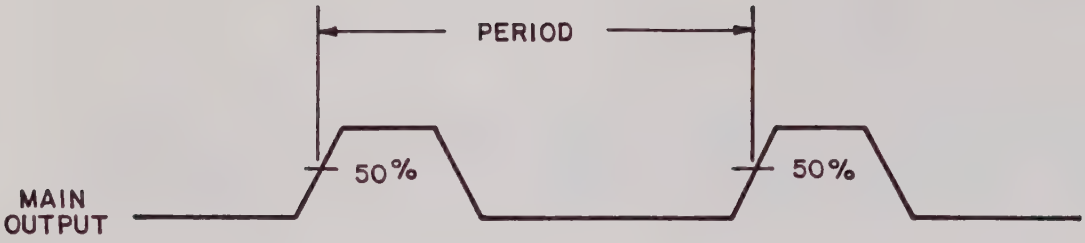


FIGURE 3-1

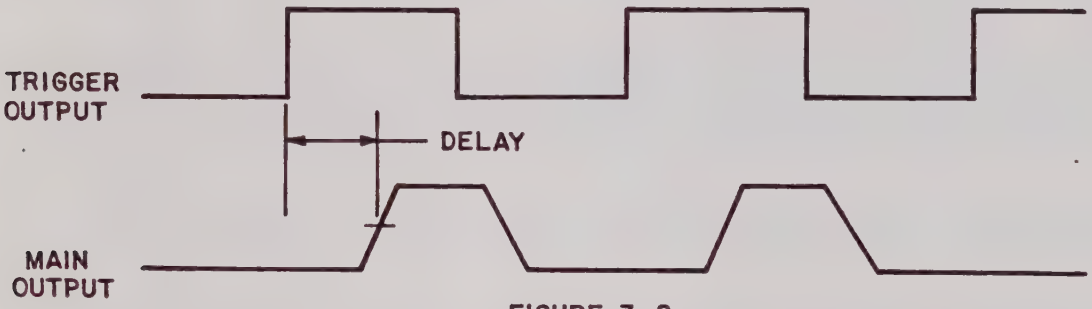


FIGURE 3-2

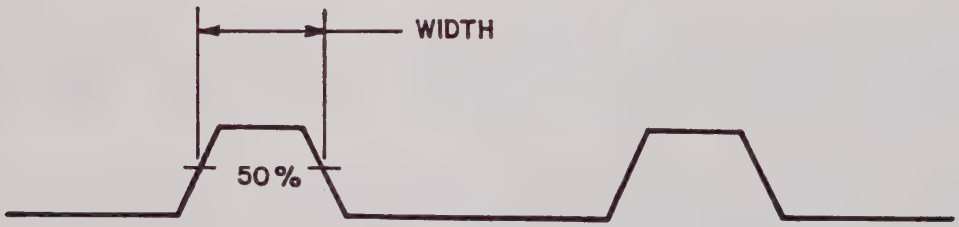


FIGURE 3-3

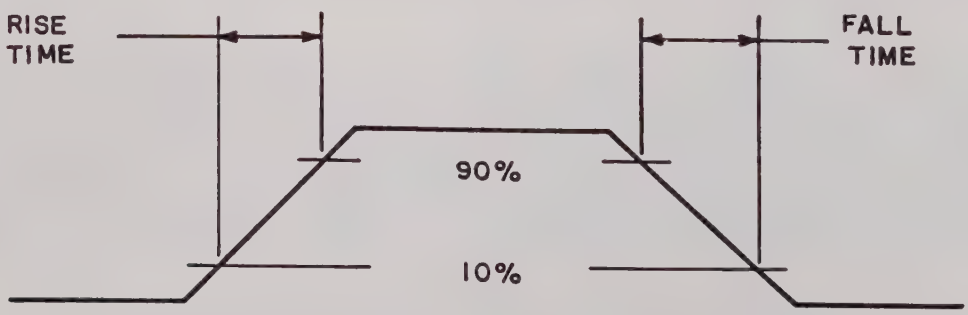


FIGURE 3-4

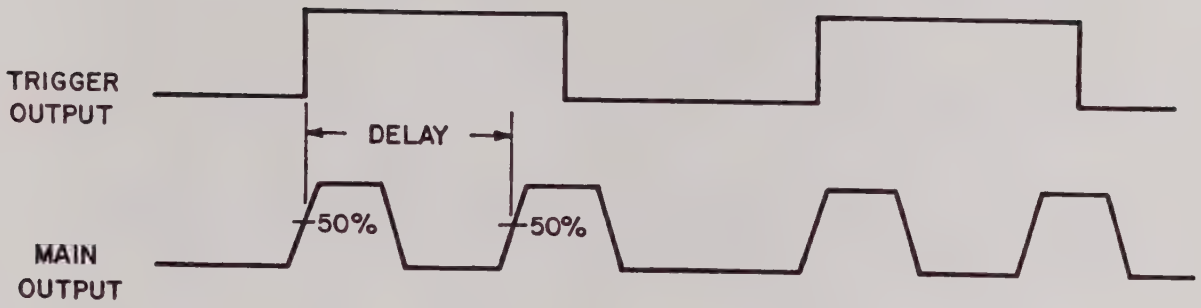


FIGURE 3-5

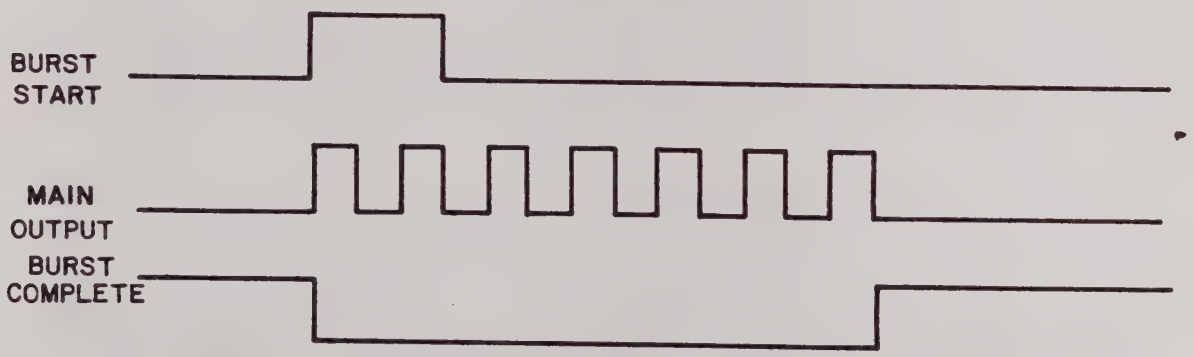


FIGURE 3-6

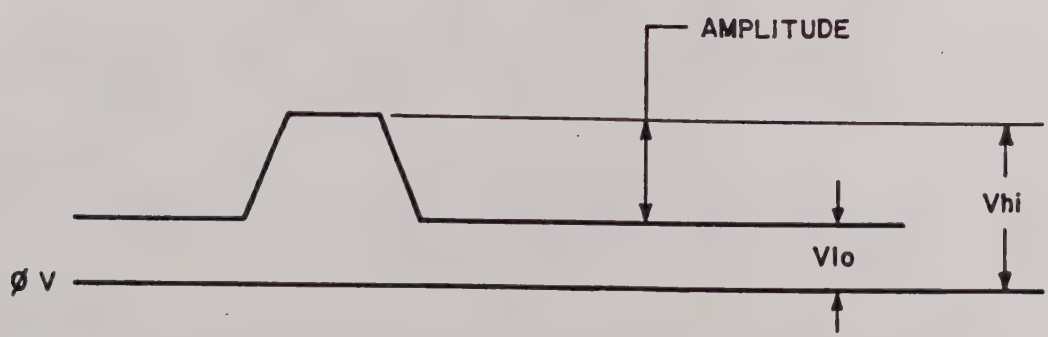


FIGURE 3-7

3. All Interface Parameters are loaded from EEPROM.
4. All Deskewing Constants are loaded from EEPROM.
5. The Protect Level is set to 1.
6. Setup number 0 becomes the active setup.
7. The CRT shows the Main Operating Display.

3.3 FRONT PANEL OPERATION

This section describes how to operate the SPG through its optional front panel.

3.3.1 CRT DISPLAY

The following numbered descriptions refer to like numbered items pointed to in Figure 3-8.

1. External CLK Trigger:

If OFF, the clock is supplied internally. If ON, the clock is supplied by an external source through J109. If the C2100 is installed the external source is supplied through J113.

1A. EXT -- ON/OFF (C2100 Clock Board)

Channel triggering status. OFF is internal. ON is external. The external inputs are J114 through J117. J109 is CLK out.

2. Internal Period:

The period of the internal clock.

3. Burst:

If ON, the unit is in the Burst mode. The burst will not start however, unless externally triggered, or the ENTER button is pressed when the cursor is on the Start parameter. If OFF, the Burst mode is disabled.

4. Count:

The number of cycles that will be completed during a burst if the Burst mode is ON. There can be 1 through 65,535 cycles.

5. Start?

Used when the Burst mode is ON. To begin the burst, the ENTER button is pressed when the cursor is on the question mark.

6. Ch

The channel number as corresponds to the channel board and output driver module in the positions 1, 2, 3 or 4. The positions are marked on the frame inside the unit.

7. Delay

The delay from the trigger output signal to the beginning of the pulse. See Appendix E for specifications regarding the measurement of the true delay.

MAIN DISPLAY SCREEN

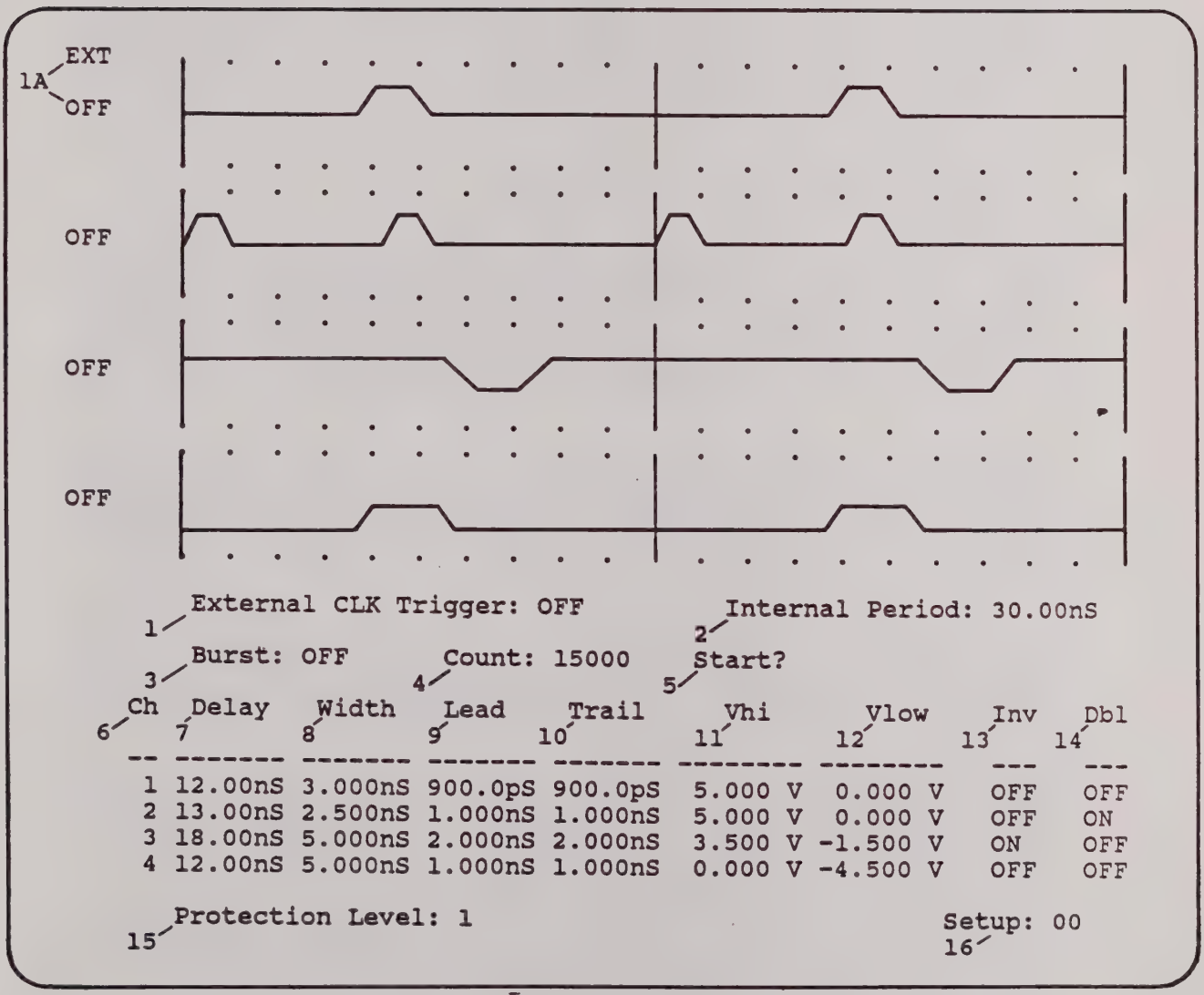


Figure 3-8

8. Width

The time for the width of the pulse.

9. Lead

The time for the leading edge of the pulse.

10. Trail

The time for the trailing edge of the pulse.

11. Vhi

The high voltage value for the pulse.

12. Vlow

The low voltage value for the pulse.

13. Inv

Indicates whether a channel is in the Inverted mode. If ON, the baseline will be at Vhi and will go to Vlo for the duration of the pulse. If OFF, the baseline will be at Vlo and will go to Vhi for the duration of the pulse.

14. Dbl

Indicates whether a channel is in the Double Pulse mode. If ON, two pulses will occur during one period. The first pulse will occur at the trigger and the second at the programmed delay time. If OFF, only one pulse will occur during a period.

15. Protection Level:

Designates the level of protection offered in the case of programmed values that are out of specification. The system comes up in the first protect level (PL 1).

PL 1 is the highest degree of protection. Any error made while programming the pulse parameters will show up as an inverted display, i.e. highlighted, or a sentence or phrase describing what is wrong. No change in the output of the unit will occur until the value is corrected.

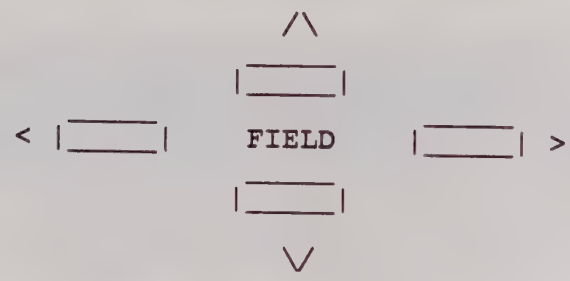
PL 2 will show an error but the unit will attempt to output a signal as close as possible to the programmed value.

PL 3 will not show an error and the unit will attempt to output the signal.

In PL 2 and 3 the operating specifications of the unit may be exceeded so the output signal should be checked to see if requirements are being met. Possible damage to the external hardware may also occur. It is recommended that PL 1 be used at all times.

16. Setup: The number of the current setup (a set of all parameter values for four channels). There are forty setups available.

3.3.2 KEYBOARD
(Refer to Figure 3-9)



moves the cursor up one line and to the beginning of a parameter.

moves the cursor down one line and to the beginning of a parameter.

moves the cursor one parameter to the left.

moves the cursor one parameter to the right.

When the field keys are used, the number where the cursor was before the key was pressed is entered and the output will change if not in the Edit mode.

---

moves the cursor one space to the left.

moves the cursor one space to the right.

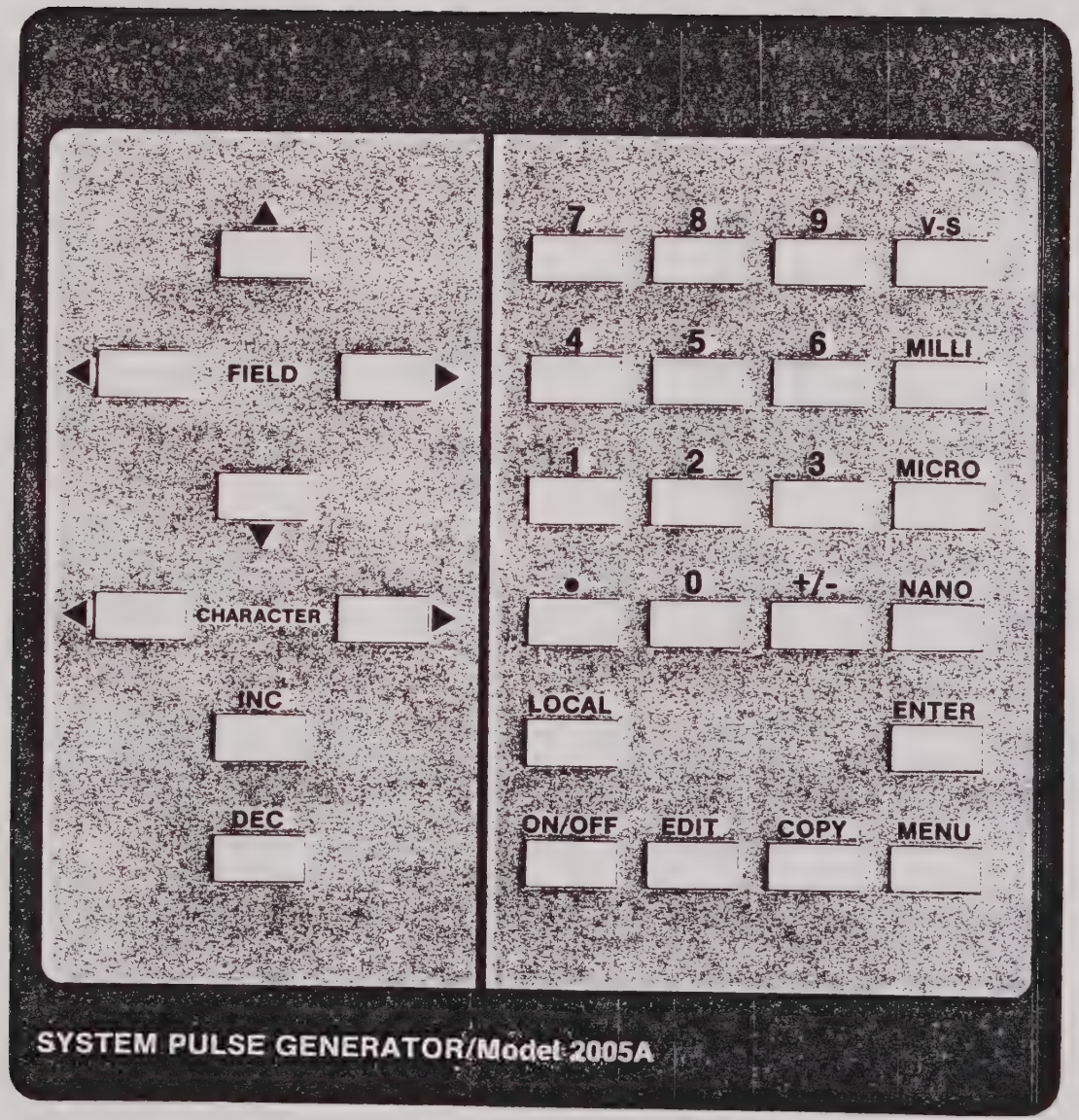
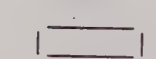

FIELD
CHARACTER
INC
DEC
7
8
9
V-S
4
5
6
MILLI
1
2
3
MICRO
•
0
+/-
NANO
LOCAL
ENTER
ON/OFF
EDIT
COPY
MENU
SYSTEM PULSE GENERATOR/Model 2005A

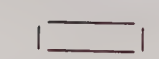
Figure 3-9

INC



increments by one the number where the cursor is.

DEC



decrements by one the number where the cursor is.

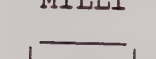
0--9

changes the value where the cursor is to the value above the button.

V-S

changes the parameter units to either volts or seconds depending on the cursor location, and enters the number to the left of the cursor.

MILLI



changes the parameter units to either millivolts or milliseconds, and enters the number to the left of the cursor.

MICRO

changes the parameter units to nanoseconds and enters the number to the left of the cursor.

NANO

changes the parameter units to nanoseconds and enters the number to the left of the cursor.

LOCAL

sets the operating mode to local.

In Local mode the parameters are controlled from the front panel.

In Remote mode the parameters are controlled from the IEEE-488 interface. In this mode, the screen display shows only the word "REMOTE" and the keyboard is locked out. The Remote mode is entered by addressing the SPG over the IEEE-488 interface.

ENTER

enters values into the registers and leaves the cursor at the beginning of the parameter.

It is also used to initiate a burst when in the Burst mode.

The ENTER key can be used to obtain a more detailed menu display. See section 3.3 for an explanation of the menu.

ON/OFF

is used for toggling ON/OFF parameters.

EDIT

toggles in and out of the Edit mode. The words "EDIT MODE" appear at the bottom of the screen when in the Edit mode.

When in the Edit mode, any change can be made on the screen and the output will not change. The output will change when the user goes out of the Edit mode.

When not in the Edit mode, any change that is made changes the output as soon as it is entered.

COPY

toggles in and out of the Copy mode. The Copy mode allows copying of channel parameters from any channel of any setup to any channel of the currently active setup. This also includes copying from channel to channel within the currently active setup. The following line will appear near the bottom of the screen when in Copy mode.

COPY from Ch X, Setup XX to Ch X, Setup XX Execute?

Use the cursor control keys to move the cursor to each of the first three parameters and change to the desired values. To initiate the actual copy process, move the cursor to the Execute? position and press ENTER. Additional copies to different channels may be made before exiting the Copy mode.

MENU

brings up the menu display if pressed when the waveform display is on the screen.

It is also used for a less detailed menu when in one of the menu categories. See section 3.3.3 for an explanation of the menu.

.

is used for entering a decimal point.

+/-

toggles between positive and negative signs.

3.3.3 MENU

When the SPG is powered on, it will display the pulse waveforms and parameters. A series of menus may be selected by pressing the MENU button which will allow the user to change other SPG settings. Figure 3-10 shows a graphic representation of the menu relationships.

When the MENU button is pressed, the screen will display the following:

```
** EH-2000 MENU **
 - Interface constants
 - Channel Setup Storage
 - T0 Deskew Constants
 - Calibration history
 - System test
 - Special Functions

Place the cursor on selection and press ENTER.
Use the MENU key to return to previous display.
```

To obtain a more detailed display of a menu item, move the cursor to the item by using the up and down field keys, then press ENTER.

NOTE: The up and down field keys are used throughout the menu to move the cursor to the desired position.

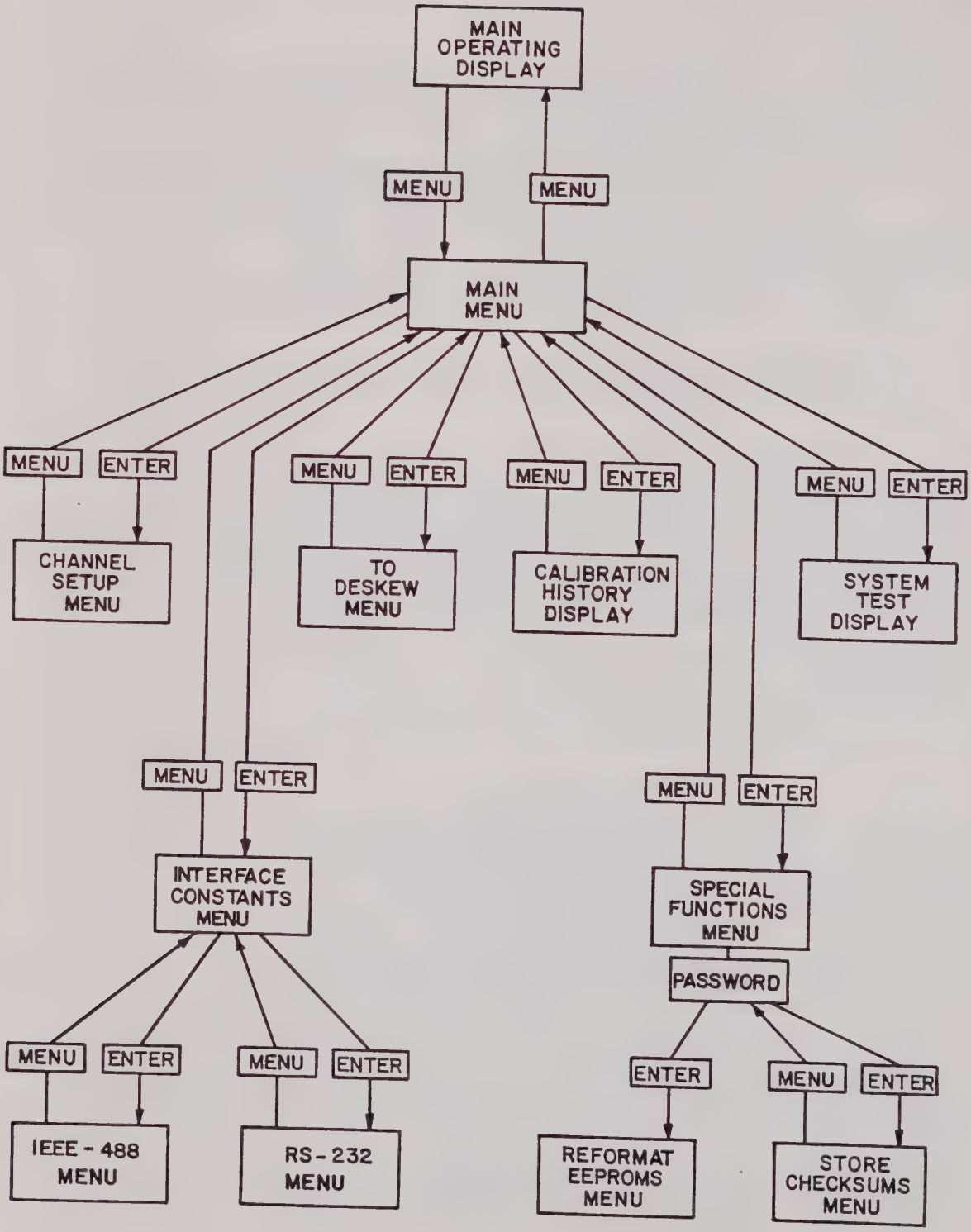

MAIN OPERATING DISPLAY
MENU
MENU
MAIN MENU
MENU
ENTER
CHANNEL SETUP MENU
MENU
ENTER
TO DESKEW MENU
MENU
ENTER
CALIBRATION HISTORY DISPLAY
MENU
ENTER
SYSTEM TEST DISPLAY
MENU
ENTER
INTERFACE CONSTANTS MENU
MENU
ENTER
IEEE - 488 MENU
MENU
ENTER
RS - 232 MENU
MENU
ENTER
SPECIAL FUNCTIONS MENU
PASSWORD
ENTER
REFORMAT EEPROMS MENU
MENU
ENTER
STORE CHECKSUMS MENU

FIGURE 3-10

3.3.3.1 INTERFACE CONSTANTS

When this line is selected, it enables the user to select IEEE-488 or RS-232 interface constants. When the interface is selected, the screen will display the appropriate constants. For IEEE-488 the screen will display the following:

```
                IEEE-488 Parameters

        SPG address (0-30)                          >
        Parallel poll bit (1-8, 0=None)             >
        Device clear set to power-up state          >
        Save to EEPROM                              >

Place cursor on selection and use INC/DEC to change.
Use the MENU key to return to previous display.
```

The values are input to the right of the arrows.

To save to the EEPROM, ENTER is pressed when the cursor is opposite "Save to EEPROM". If the values are not saved, they will only be in effect until the power is turned off.

When RS-232 is selected, the screen will display the following:

```
                RS-232 Parameters

        Baud rate                                   >
        Number of data bits (5,6,7,8)               >
        Number of stop bits (1,1.5,2)               >
        Parity (odd,even,none)                      >
        Save to EEPROM                              >

   Place cursor on selection and use INC/DEC to change
   Use the MENU key to return to previous display
```

The values are input to the right of the arrows.

To save to the EEPROM, ENTER is pressed when the cursor is opposite "Save to EEPROM". If the values are not saved, they will only be in effect until the power is turned off.

3.3.3.2 CHANNEL SETUP STORAGE

When this line is selected, the screen will display the following:

```
                Channel Setup Storage

  Restore channel setups to power-up state     >

  Save first five channel setups to EEPROM     >

  NOTE:  Restoring channel setups affects only
         the first five setups.

         Only the first five channel setups may
         be saved to EEPROM.

  Place cursor on selection and press ENTER
  Use the MENU key to return to previous display
```

Values for these 5 setups are programmed initially at the factory. Copying the setups to permanent storage will erase the factory values and store whatever values are in the registers. Restoring the setups to the power up state brings the setups to the values last stored regardless of changes made to the front panel.

For storage of all 40 setups, values can be stored remotely through one of the interfaces to be recovered at a later time.

3.3.3.3 T0 DESKEW CONSTANTS

When this line is selected, the screen will display the following:

```
T0 Deskewing Constants

Ch 1        > X.XXX S
Ch 2        > X.XXX S
Ch 3        > X.XXX S
Ch 4        > X.XXX S

Save to EEPROM

Use the MENU key to return to previous display
```

Deskewing constants specify an additional set of values which offset each channel's output pulse from the common trigger output. These values correct for the offset caused primarily by test hardware such as varying cable lengths and fixture capacitance. Deskewing constants allow all channels to arrive at the desired points at the time indicated by the Delay parameters. Once the deskewing parameters have been entered, the operator is freed from having to consider the effects of hardware delays on his programming parameters. Note however, that the sum of the deskewing constant plus the programmed delay for any given channel may not exceed the specifications of the SPG.

The limits for the deskewing constants are 0 - 5 n sec.

To save to the EEPROM, ENTER is pressed when the cursor is opposite "Save to EEPROM". If the values are not saved, they will only be in effect until the power is turned off.

3.3.3.4 CALIBRATION HISTORY

When this line is selected, the screen will display the following:

```
                                  Ser#      Cal Date
            Clock Bd.             XXXX      MMDDYY
      N V   Channel 1             XXXX      MMDDYY
      N V   Channel 2             XXXX      MMDDYY
      N V   Channel 3             XXXX      MMDDYY
      N V   Channel 4             XXXX      MMDDYY

   Use the MENU key to return to previous display
```

"N" will be the maximum voltage rating of the channel, ex. 5 V.

This history is stored in EEPROMs located on the clock and channel boards.

3.3.3.5 SYSTEM TEST

When this line is selected, the screen will display the following:

```
          System Test - SPG vers X.X

             ROM 0 Checksum        >
             ROM 1 Checksum        >
             ROM 2 Checksum        >
             ROM 3 Checksum        >
             Clock ROM Checksum    >
             Channel 1 Checksum    >
             Channel 2 Checksum    >
             Channel 3 Checksum    >
             Channel 4 Checksum    >
             EEPROMS Checksum      >
             System RAM 0          >
             System RAM 1          >
             System RAM 2          >
             System RAM 3          >
             Display RAM 0         >
             Display RAM 1         >
             CRT Controller        >
             Clock Chain           >
             Timer                 >
             Math Processor        >

  Use the MENU key to return to previous display
```

The System Test is executed at power-up, from the Menu, or from a command over one of the remote interfaces. A PASS or FAIL indication will follow each of the tests listed above.

The following is a brief description of each of the tests performed:

ROM 0 through ROM 3 Checksum	The sums of these four ROMs located on the CPU board are compared against the values stored in EEPROM.
Clock ROM Checksum	The checksum of the ROM located on the Clock Board is compared against the value stored in EEPROM. See note below.
Channel 1 through 4 Checksum	The checksum of the ROMs located on each of the channel boards are compared against the values stored in EEPROM. See note below.
EEPROMS Checksum	The checksum of the EEPROMs located on the CPU board are compared against the values stored in EEPROM. These values are updated each time the contents of the EEPROMs are changed.
System RAM 0 through 4	The four RAMs located on the CPU board are tested non-destructively.
Display RAM 0 and 1	The two RAMs located on the CRT Controller board are tested non-destructively.
CRT Controller	The CRT Controller is functionally tested.
Clock Chain	The Clock Chain is functionally tested.
Timer and Math Processor	The Math Processor and Timer are functionally tested.

NOTE: If a Clock Board or a Channel Board is replaced in the SPG, the checksum test for that board will fail because of its different calibration data. See Section 3.3.3.6 for the method of correcting this situation.

3.3.3.6 SPECIAL FUNCTIONS

When this line is selected, the screen will display the following:

```
Please enter password:

Use the MENU key to return to the previous display
```

The password is available upon the request of an authorized representative of the company to which the unit is sold. It is intended to prevent tampering with the configuration of unit except by those with need, i.e., cal lab, etc.

Pressing the ENTER key after the password is entered will give the following display:

```
Special Function

Save checksums to EEPROM    >
Reformat EEPROM             >
Multiple Ext Clk: Toggle?   >

Place cursor on selection and press ENTER
Use the MENU key to return to the previous display
```

The following is a brief description of each function above:

Save checksums to EEPROM — The checksums of the clock board and all channel boards are stored in the EEPROM when the ENTER key is pressed. Checksums formerly in the EEPROM are erased. See section 3.4.4.4 -- SAVECS.

Reformat EEPROM — Erases and reformats the EEPROMs on the microprocessor board. The 'Save checksums' routine must be performed after this function.

Multiple Ext Clk: Toggle? — Two versions of the clock board are available. This function allows the use of either clock with this firmware revision. Hardware restrictions prevent the interchange of the boards except at the factory.

3.4 REMOTE OPERATION

This section describes each of the remote commands which may be sent to the SPG from either the IEEE-488 or the RS-232 interface. The same syntax is used with either interface.

3.4.1 COMBINING COMMANDS

Individual commands may be grouped into complete messages by separating each command from the next with a semi-colon (;). This gives the system controller the ability to change all desired pulse parameters in a single output statement.

EXAMPLE: The message PER:100n;WID:35n,1;DLY:15n,1 would set the period to 100 nSec and would set the channel one output to a width of 35 nSec after a delay of 15 nSec.

3.4.2 MESSAGE TERMINATORS

Each complete message sent to the SPG must be terminated in one of several ways to indicate the end of tranmission. A line-feed character (ASCII code 10 decimal) may be sent by either interface as a terminator. A carriage-return (ASCII code 13 decimal) and line-feed sequence may also be used. In addition, the EOI (End Or Identify) line of the IEEE-488 interface may also be used as a message terminator.

All commands ending with a question mark (?) will cause the SPG to return a data message over the interface to the controller. All messages sent over the IEEE-488 interface from the SPG to the controller will be terminated by a single line-feed character coincident with the EOI line going true. Messages sent over the RS-232 interface from the SPG to the controller will be terminated by a carriage-return and line-feed sequence.

3.4.3 ERROR REPORTING

The SPG scans all commands for errors before execution. Once a syntax error or missing argument error is detected, the remainder of the command is ignored. That is, only that part of the command up to the point error is executed. Parts of a command that are simply out of range or incompatible with other parameters do not cause the remainder of the command to be ignored. Regardless of the type of error detected, the SPG will report the error to the controller in one of two ways depending on which interface is being used.

3.4.3.1 RS-232

The SPG will send a message to the controller as soon as an error is detected. One of the following three messages will be sent:

Syntax Error	[sent whenever a non-valid command name is received]
Missing argument	[sent when a required parameter is missing from the command]

Program error [sent whenever a parameter is out of it's valid range]

All error messages will be terminated by a carriage-return and line-feed sequence.

3.4.3.2 IEEE-488 INTERFACE

The SPG will indicate an error condition to the controller by the following three procedures. No actual message will be sent by the SPG.

1. Upon detection of an error, the SPG will assert the Service Request (SRQ) line of the IEEE-488 interface. This line will stay active until either a Serial Poll is performed on the SPG or until another valid command is sent and no more errors are present.

2. Detection of an error will cause the SPG to assert a previously selected bit during a Parallel Poll. A Parallel Poll is performed by sending the Parallel Poll Enable (PPE) message over the interface. The bit to be asserted is selected by the SPG's PPLBIT n command. If n is set to 0, then none of the bits are asserted, and therefore detection of an error is not possible using a Parallel Poll. The selected bit (if any) will stay active during subsequent Parallel Polls until either a Serial Poll is performed on the SPG or until another valid command is sent and no more errors are present.

3. Detection of an error will cause the SPG to return a non-zero byte during a Serial Poll. A Serial Poll is performed by sending a Serial Poll Enable (SPE) message over the IEEE-488 interface. One of the following nine decimal values will be sent depending on the type of error which occurred:

65	[Syntax error]
66	[Missing argument error]
67	[Period out of range]
68	[Channel 1 parameters out of range: LED and TED edges on different ranges or VHI and VLO incompatible]
69	[Same as 68 except for Chan 2]
70	[Same as 68 except for Chan 3]
71	[Same as 68 except for Chan 4]
72	[Channel 1 parameters are incompatible with period]
73	[Same as 72 except for Chan 2]

74 [Same as 72 except for Chan 3]

75 [Same as 72 except for Chan 4]

A Serial Poll of the SPG will reset the SRQ line of the IEEE-488 interface, clear the Parallel Poll response bit, and return the Serial Poll byte to a zero value. A valid command to the SPG will also clear these same items provided that no remaining errors are present.

3.4.4 COMMAND SYNTAX

All command names sent to the SPG may be in either upper or lower case characters. Each command name must be separated from any following parameters by a colon (:) or a space.

The following conventions are used throughout the list of command names:

[ ]	brackets indicate an optional parameter.
/	a slash indicates a choice of one parameter.
c	indicates an integer channel number from 1 through the number of channel cards currently installed.
n	indicates an integer value within the valid range.
v	indicates a floating point value within the valid range.
u	indicates one of the following measurement units. Upper or lower case characters may be used.

p for picoseconds.
n for nanoseconds.
u for microseconds.
m for milliseconds or millivolts.
for seconds or volts.

NOTE: No character is used to indicate seconds or volts since time or amplitude will be determined by the command name itself.

3.4.4.1 COMMANDS AFFECTING ALL CHANNELS

EXTTRIG:ON/OFF
(Firmware Rev. 1.6 & above)

Sets the external trigger of the SPG either on or off. If OFF, the period of all channels will be set by the PER command. If ON, the period is determined by the signal input at the rear panel CLOCK IN connector J113. (J109 on earlier models)
EXAMPLES: EXTTRIG:ON
EXTTRIG:OFF

INTTRIG:ON/OFF (Firmware Rev. 1.5 & Below)	Sets the internal trigger of the SPG either on or off. If ON, the period of all channels will be set by the PER command. If OFF, the period is determined by the signal input at the rear panel CLOCK IN connector, J109.
PER:vu	Sets the period of the internal clock to the desired time interval. The time defined by vu must be within the valid range of period for the SPG. EXAMPLES: PER:123n PER:.123u
BURSTCT:n	Sets the number of pulses that will be output during each burst. n may range from 1 thru 65535. This command does not actually enable or initiate the burst itself. EXAMPLES: BURSTCT:5 BURSTCT:12345
BURSTCT:ON/OFF	Enables or disables the Burst mode. Once BURST:ON has been sent, all subsequent BURSTGO commands will initiate a burst as defined by the BURSTCT command. No bursts will occur if BURST:OFF has been sent. EXAMPLES: BURST:ON BURST:OFF
BURSTGO	Initiates a burst if burst mode has been previously enabled by using the BURST ON command. The length of the burst must have been previously defined in a BURSTCT command. The IEEE-488 interface can also start a burst by sending the Group Execute Trigger (GET) message. In addition, a signal to the rear panel BNC connector J109 (Burst Start) will also initiate a burst. EXAMPLE: BURSTGO

3.4.4.2 COMMANDS AFFECTING ONLY ONE CHANNEL

CH:c

Selects the default channel for all subsequent channel commands. Unless an optional channel parameter is added to these commands, the default channel as specified in this command will be used. The parameter c may not exceed the number of channel boards installed in the SPG. The SPG defaults to CH:1 at power up.

EXAMPLES: CH:1 and CH:4

CHTRIG:ON/OFF[,c]
(C2100 Clock Board Only)

Selects the trigger source for the channel board given by the number 'c'. Internal source is selected with OFF. ON will select an external source at the corresponding rear panel CHAN c IN connector, J114-J117. If no channel number is used, the default is to channel 1.

EXAMPLES: CHTRIG:ON,1
CHTRIG:OFF,3

DLY:vu[,c]

Sets the delay from the trigger output to the start of the pulse on the desired channel. In Double Pulse Mode, the DLY command sets the delay between the first and second pulse in each period. If the optional channel parameter is omitted, the default channel number will be used.

EXAMPLES: DLY:36n
DLY:40u,3

WID:vu[,c]

Sets the pulse width of the desired channel. If the optional channel parameter is omitted, the default channel number will be used.

EXAMPLES: WID:10.5u
WID:.5m,1

LED:vu[,c]

Sets the leading edge time of the pulse on the desired channel. Leading edge time is defined from 10% to 90% of pulse amplitude. If the optional channel parameter is omitted, the default channel number will be used.

EXAMPLES: LED:5u
LED:1500p,2

TED:vu[,c]

Sets the trailing edge time of the pulse on the desired channel. Trailing edge time is defined from 90% to 10% of pulse amplitude. If the optional channel parameter is omitted, the default channel number will be used.

EXAMPLES: TED:12n and TED:5.U,4

VHI:vu[,c]

Sets the voltage level of the output pulse during its active portion as defined by the WID command. The value defined by vu must be within the valid range defined for the particular model of SPG being programmed. The numerical value of VHI must always be greater than VLO. If the optional channel parameter is omitted, the default channel number will be used.

EXAMPLES: VHI:4
VHI:-123m,2

VLO:vu[,c]

Sets the voltage level of the output pulse during its baseline or inactive portion. The value defined by vu must be within the valid range defined for the particular model of SPG being programmed. The numerical value of VLO must always be less than VHI. If the optional channel parameter is omitted, the default channel number will be used.

EXAMPLES: VLO:-2.6
VLO:100m,1

ZEROCHAN:[c]

Used to set the channel (c) output to 0 volts.

DBL:ON/OFF[,c]

Enables or disables the Double Pulse Mode on the desired channel. If OFF, only one pulse per period is output. If ON, two pulses of identical waveshape are output per period with the second pulse delayed from the first by the value defined in the DLY command. If the optional channel parameter is omitted, the default channel number will be used.

EXAMPLES: DBL:ON
DBL:OFF,3

INV:ON/OFF[,c]

Enables or disables the Invert Mode on the desired channel. If OFF, the pulse baseline will be at VLO and the pulse will go to the VHI level for the time specified by WID. If ON, the pulse baseline will be at VHI and the pulse will go to the VLO level for the time specified by WID. Invert mode may be combined with Double Pulse Mode. If the optional channel parameter is omitted, the default channel number will be used.

EXAMPLES: INV:ON,2
INV:OFF

TØ:vu[,c]

Sets the deskewing delay from the trigger output to the start of the pulse for the desired channel. If the optional channel parameter is omitted, the default channel number will be used.

EXAMPLES: TØ:2.5n
TØ:3n,2

COPY:c1,n,c2

Copies channel c1 parameters from setup n to channel c2 of the current setup.

EXAMPLES: COPY:3,27,1
COPY:2,10,2

3.4.4.3 INTERFACE CONTROL COMMANDS

PPLBIT:n

Sets the active Parallel Poll bit on the IEEE-488 Bus. This bit (1-8) will be asserted in response to a Parallel Poll Enable command from the System Controller only if the SPG has requested service by way of the SRQ line. If n is set to 0, then none of the bits will be set.

EXAMPLES: PPLBIT:1
PPLBIT:8

DEVICE:n

Sets the IEEE-488 device address of the SPG. n may range from 0 through 30.

EXAMPLES: DEVICE:5
DEVICE:30

PONCLR:ON/OFF

Sets the response of the SPG to the IEEE-488 Device Clear (DCL) and Selected Device Clear (SDC) messages. If set to ON, the SPG will include restoration of the first five setups to the power-on state as part of its clearing function. If set to OFF, the first five setups will not be restored to the power-on state.

EXAMPLES: PONCLR:ON
PONCLR:OFF

SAVE488

Saves all IEEE-488 parameters to EEPROM.

EXAMPLE: SAVE488

BAUD:n

Sets the baud rate of the RS-232 interface. The following numbers are valid values for n: 110, 300, 1200, 2400, 4800, 9600, and 19200.

EXAMPLES: BAUD:300
BAUD:9600

DATA:n

Sets the number of data bits used on the RS-232 interface. The value n must be 5, 6, 7, or 8.

EXAMPLES: DATA:7
DATA:5

STOP:n

Sets the number of stop bits used on the RS-232 interface. The value n must be 1, 1.5, or 2.

EXAMPLES: STOP:1
STOP:2

PARITY:ODD/EVEN/NONE

Sets the type of parity used on the RS-232 interface.

EXAMPLES: PARITY:ODD
PARITY:NONE

SAVE232

Saves all RS-232 parameters to EEPROM.

EXAMPLE: SAVE232

3.4.4.4 MISCELLANEOUS COMMANDS

EDIT:ON/OFF

Enters or exits the Edit mode. If set to ON, the Edit mode will allow changes to be made to all parameters without the actual pulse outputs changing. All pulse outputs will then be updated to the current parameters when the Edit mode is exited by sending OFF.

EXAMPLES: EDIT:ON
EDIT:OFF

SET:n

Selects one of the forty stored setups and updates all pulse parameters to the stored values. n must be in the range 0 through 39.

EXAMPLES: SET:0
SET:39

SAVETBLS

Saves setups 0 through 4 into EEPROM for permanent storage. These five setups will then be present after the next power-up cycle.

EXAMPLE: SAVETBLS

LOADTBLS	Load setups 0 through 4 from EEPROM. This operation is automatically done during power up, but it can also be used to restore the first five setups to the power up state at any time. EXAMPLE: LOADTBLS
SAVET0	Saves the present TØ delay value of each channel to EEPROM for permanent storage. EXAMPLE: SAVET0
PROTECT:n	Sets the error protect mode to n, where n may be a value 1 through 3 as described in the Front Panel Operation section. EXAMPLES: PROTECT:1 PROTECT:3
RESET	Causes the firmware to jump to the start of its program. EXAMPLE: RESET
SAVECS: [password]	Stores the checksums of the clock board and all channel boards in the EEPROM. EXAMPLE: SAVECS: xxxxx
NEWEE: [password]	Reformats the EEPROMs. SAVECS must be executed immediately after this command. EXAMPLE: NEWEE: xxxxx
CLKTYP: [password]	Toggle the software key used to determine the type of clock board in the unit. See section 3.3.3.6 - Save checksums'. EXAMPLE: CLKTYP: xxxxx

3.4.4.5 COMMANDS WHICH RETURN DATA FROM THE SPG

EXTTRIG?

Returns the state of the external trigger. The word ON or OFF will be returned to the controller.

EXAMPLE: EXTTRIG?
returns: ON (ext. triggered)
or: OFF (int. triggered)

CHTRIG?
(C2100 Clock only)

Returns the state of all of the external channel trigger sources.

EXAMPLE: CHTRIG?
returns: 1-ON:2-OFF:3-OFF:4-ON

PER?

Returns the period of the internal clock.

EXAMPLE: PER?
returns: 23.70n

BURSTCT?

Returns the number of pulses programmed for each burst.

EXAMPLE: BURSTCT?
returns: 5

BURST?

Returns the state of the Burst mode. The word ON or OFF will be returned to the controller.

EXAMPLE: BURST?
returns: ON

CH?

Returns the default channel number to be used in all channel related commands unless explicitly stated otherwise.

EXAMPLE: CH?
returns: 1

DLY?[:c]

Returns the delay value for the desired channel. If the optional channel parameter is omitted, the default channel number will be used.

EXAMPLES: DLY?
or: DLY?:2
returns: 5.600n

WID?[:c]

Returns the width value for the desired channel. If the optional channel parameter is omitted, the default channel number will be used.

```
EXAMPLES:  WID?
      or:  WID?:3
 returns:  234.0n
      or:  56.00m
```

LED?[:c]

Returns the leading edge value for the desired channel. If the optional channel parameter is omitted, the default channel number will be used.

```
EXAMPLES:  LED?
      or:  LED?:4
 returns:  1.000u
      or:  12.40n
```

TED?[:c]

Returns the trailing edge value for the desired channel. If the optional channel parameter is omitted, the default channel number will be used.

```
EXAMPLES:  TED?
      or:  TED?:1
 returns:  45.60u
      or:  2.400n
```

VHI?[:c]

Returns the VHI value for the desired channel. If the optional channel parameter is omitted, the default channel number will be used.

```
EXAMPLES:  VHI?
      or:  VHI?:2
 returns:  2.340
      or:  -534.0m
```

VLO?[:c]

Returns the VLO value for the desired channel. If the optional channel parameter is omitted, the default channel number will be used.

```
EXAMPLES:  VLO?
      or:  VLO?:3
 returns:  -1.500
      or:  300.0m
```

DBL?[:c]

Returns the state of the Double Pulse Mode for the desired channel. The word ON or OFF will be returned. If the optional channel parameter is omitted, the default channel number will be used.

```
EXAMPLES:  DBL?
      or:  DBL?:1
 returns:  ON
      or:  OFF
```

INV?[:c]

Returns the state of the Invert Mode for the desired channel. The word ON or OFF will be returned. If the optional channel parameter is omitted, the default channel number will be used.

```
EXAMPLES:  INV?
      or:  INV?:4
 returns:  ON
      or:  OFF
```

TØ?[:c]

Returns the value of the TØ delay for the desired channel. If the optional channel parameter is omitted, the default channel number will be used.

```
EXAMPLES:  TØ?
      or:  TØ?:2
 returns:  3.500n
      or:  4.000n
```

GETCHAN?[:c]

Returns the complete programmed values for one channel in the present setup. If the optional channel parameter is omitted, the default channel number will be used. This command gives the SPG the ability to send a string to the controller that may be recalled later in order to duplicate the present setup.

```
EXAMPLES:  GETCHAN?
      or:  GETCHAN?:3
```

returns: CH:1;DLY:10.00n;WID:
10.00n;LED:5.000n;TE
D:1.250n;VHI:2.500;V
LO:1.000;DBL:OFF;INV
:ON

PPLBIT?

Returns the value of the Parallel Poll Bit on the IEEE-488 bus. The value returned will be 0 through 8.

EXAMPLE: PPLBIT?
returns: 1
or: 8

DEVICE?

Returns the device address on the IEEE-488 bus. The value returned will be 0 through 30.

EXAMPLE: DEVICE?
returns: 5
or: 27

PONCLR?

Returns the state of the Power-On-Clear flag. The word ON or OFF will be returned.

EXAMPLE: PONCLR?
returns: ON
or: OFF

BAUD?

Returns the RS-232 baud rate. The returned value will be 110, 300, 1200, 2400, 4800, 9600, or 19200.

EXAMPLE: BAUD?
returns: 300
or: 9600

DATA?

Returns the number of data bits used with the RS-232 interface. The returned value will be 5, 6, 7, or 8.

EXAMPLE: DATA?
returns: 5
or: 8

STOP?

Returns the number of stop bits used with the RS-232 interface.

The returned value will be 1, 1.5, or 2.

EXAMPLE: STOP?
returns: 2
or: 1

PARITY?

Returns the parity used with the RS-232 interface. The returned word will be NONE, EVEN, or ODD.

EXAMPLE: PARITY?
returns: EVEN
or: NONE

SET?

Returns the current setup number. The value returned will be in the range 0 through 39.

EXAMPLE: SET?
returns: 2
or: 29

CALHIST?

Returns the serial numbers and calibration dates (month, day, year) for the clock board and each of the installed channel boards.

EXAMPLE: CALHIST?
returns: CLK SER#1234, 013084
CH1 SER#2345, 020184
CH2 SER#3456, 123183
CH3 SER#4567, 090184
CH4 SER#4568, 090184

SYSTEST?

Executes a system test and returns the status of any test which failed, if any. A test heading and a completion message are always sent regardless of any failures.

EXAMPLE: SYSTEST?
returns:

SYSTEM TEST - SPG VERS X.X
CLOCK CHAIN FAILED
SYSTEM TEST COMPLETE

PROTECT?

Returns the current error protect mode. The value will be 1, 2, or 3.

EXAMPLE: PROTECT?
returns: 1
or: 3

CLKTYP?

Returns the clock board type installed in the unit. 'M' is for the multiple external clock type and 'S' for the single external clock type. Refer to section 3.3.3.6 - Multiple Ext Clk: Toggle?.

EXAMPLE: CLKTYP?
returns: M
or: S

MODEL SPG2000

SECTION 4

APPENDICES

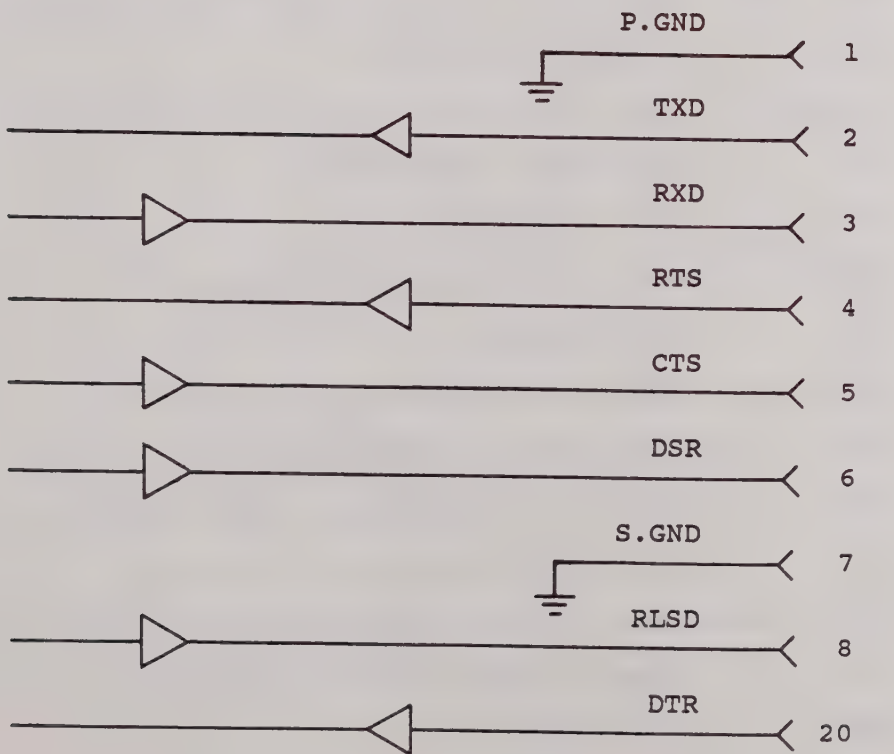
APPENDIX A

RS-232-C INTERFACE CONNECTOR (J105)
(wired for DCE operation)

PIN#	SIGNAL NAME
1	PROTECTIVE GROUND
2	TRANSMITTED DATA
3	RECEIVED DATA
4	REQUEST TO SEND
5	CLEAR TO SEND
6	DATA SET READY
7	SIGNAL GROUND
8	RECEIVED LINE SIGNAL DETECTOR
20	DATA TERMINAL READY

NOTE: All other pins are open.

RS-232-C INTERNAL DRIVER/RECEIVER CIRCUITS



APPENDIX B

IEEE-488 INTERFACE CONNECTOR (J106)

The following signal leads conform to the IEEE-488-1978 standard. All signals are low true.

PIN#	IEEE-488 MNEMONIC	SIGNAL NAME
1	DIO1	DATA INPUT/OUTPUT BIT 1 (LSB)
2	DIO2	DATA INPUT/OUTPUT BIT 2
3	DIO3	DATA INPUT/OUTPUT BIT 3
4	DIO4	DATA INPUT/OUTPUT BIT 4
5	EOI	END OR IDENTIFY
6	DAV	DATA VALID
7	NRFD	NOT READY FOR DATA
8	NDAC	NOT DATA ACCEPTED
9	IFC	INTERFACE CLEAR
10	SRQ	SERVICE REQUEST
11	ATN	ATTENTION
12	SHIELD	OVERALL CABLE SHIELD
13	DIO5	DATA INPUT/OUTPUT BIT 5
14	DIO6	DATA INPUT/OUTPUT BIT 6
15	DIO7	DATA INPUT/OUTPUT BIT 7
16	DIO8	DATA INPUT/OUTPUT BIT 8 (MSB)
17	REN	REMOTE ENABLE
18	GND	SIGNAL GROUND RETURN OF DAV (PIN 6)
19	GND	SIGNAL GROUND RETURN OF NRFD (PIN 7)
20	GND	SIGNAL GROUND RETURN OF NDAC (PIN 8)
21	GND	SIGNAL GROUND RETURN OF IFC (PIN 9)
22	GND	SIGNAL GROUND RETURN OF SRQ (PIN 10)
23	GND	SIGNAL GROUND RETURN OF ATN (PIN 11)
24	GND	LOGIC GROUND

IEEE-488 FUNCTION SUBSETS

FUNCTION	SUBSET	CAPABILITY
SOURCE HANDSHAKE Controls the initiation and termination of asynchronous multiline message transfers.	SH1	COMPLETE
ACCEPTOR HANDSHAKE Controls the transfer rate of asynchronous multiline messages.	AH1	COMPLETE
TALKER Sends device dependent data to other devices when addressed to talk.	T6	COMPLETE
EXTENDED TALKER Adds secondary addressing to talker.	TE0	NONE
LISTENER Receives device dependent data from other devices when addressed to listen.	L4	COMPLETE
EXTENDED LISTENER Adds secondary addresssing to listener.	LE0	NONE
SERVICE REQUEST Requests service asynchronously from the controller in charge.	SR1	COMPLETE
REMOTE/LOCAL The device communicates over the interface or with the front panel controls.	RL1	COMPLETE
PARALLEL POLL Capability to send a Parallel Poll Response message to the controller in charge without being previously addressed to talk.	PP2	COMPLETE
DEVICE CLEAR Able to be cleared either individually or as part of a group of devices.	DC1	COMPLETE

DEVICE TRIGGER Able to have its operation started individually or as part of a group of devices.	DT1	COMPLETE
CONTROLLER Sends device addresses, universal commands, and addressed commands to other instruments.	C0	NONE

NOTE: For additional information, refer to the IEEE Instrumentation and Measurements Group, "Standard Digital Interface for Programmable Instrumentation" Standard 488-1978 : Institute of Electrical and Electronic Engineers, July 25, 1980.

ALPHABETICAL LISTING OF REMOTE COMMAND NAMES

BAUD?
BURST
BURST?
BURSTCT
BURSTCT?
BURSTGO
CALHIST?
CH
CH?
CHTRIG
CHTRIG?
CLKTYP
CLKTYP?
COPY
DATA
DATA?
DBL
DBL?
DEVICE
DEVICE?
DLY
DLY?
EDIT
GETCHAN?
EXTTRIG
EXTTRIG?
INV
INV?
LED
LED?
LOADTBLS
NEWEE
PARITY
PARITY?
PER
PER?
PONCLR
PONCLR?
PPLBIT
PPLBIT?
PROTECT
PROTECT?
RESET
SAVE232
SAVE488
SAVECS
SAVET0
SAVETBLS
SET
SET?
STOP
STOP?
SYSTEST?
TØ
TØ?
TED
TED?
VHI
VHI?
VLO
VLO?
WID
WID?
ZEROCHAN

APPENDIX E

SPG2000 SERIES SPECIFICATIONS

PULSE REPETITION PERIOD (FREQUENCY)	5 nSec. to 1 Sec. (10 nSec at 10 V) (200 MHz to Hz; 100 Mhz at 10 V) Internal clock, continuously variable.
PULSE DELAY	Programmable from 2 nS to 26 uS, 1 Sec. with range extender option. Typical delay from T0 to leading edge of first pulse in double pulse mode = approx. 14 nS. (C2100 Clock = 0 nS $\pm$ 2 nS.) Delay is not guaranteed to exceed 50% of the period.
PULSE WIDTH	Programmable from 2 nS to 26 uS, 1 Sec. with range extender option. (4 nS minimum at 10 V). (See Section 3.1 - Width) Width not guaranteed to exceed 50% of the period.
DUTY FACTOR	$\leq$50% applies to delay and width settings. Effective duty factors approaching 100% in inverted mode.
OUTPUT PULSE AMPLITUDE	Pulse amplitude is adjusted by setting VHi and VLo and is the difference between the VHi and VLo settings.
(5 VOLT OUTPUT CHANNEL) (MODEL P2005)	VHi-VLo: 313mV to 5.0V into 50 ohms, backmatched. VHi: -5.0V to +10.0V into 50 ohms. VHi is the most positive level of the output pulse. VLo: -10.0V to +7.5V into 50 ohms. VLo is the most negative level of the output pulse. Offset affects minimum pulse amplitude. (See VHi - VLo ranges.)
(10 VOLT OUTPUT CHANNEL) (MODEL P2010)	VHi-VLo: 625 mV to 10.0V into 50 ohms, backmatched. VHi: -5.0V to +15.0V into 50 ohms. VHi is the most positive level of the output pulse. VLo: -15.0V to +10.0V into 50 ohms. VLo is the most negative level of the output pulse. Offset affects minimum pulse amplitude. (See VHi - VLo ranges.)
VHi - VLo RANGES	See Note 5-1 (Section 5)

RISE AND FALL TIMES	<1.0 nSec. to 2.0 uSec. at 5V, <2.0 nSec. to 2.0 uSec. at 10V, measured from the 10% to the 90% amplitude points.
BURST MODE	1 to 65535 pulses per burst.
BURST START, INPUT	TTL compatible, positive edge triggered.
BURST COMPLETE, OUTPUT	Output is +1.0 V into 50 ohms when burst is complete. Output is 0 V for duration of burst.
EXTERNAL CLOCK DRIVE INPUT	Positive edge triggered. Input must go from <+0.3V to >+1.0V into 50 ohms. Maximum input level is +2.5 volts. Trigger frequency is 0-200 MHz.
EXT. CHANNEL DRIVE INPUTS (C2100 CLOCK BOARD)	ECL level inputs. -0.9 V to -1.6 V typ. 0 V and -2.0 V max. Trigger freq. is 0-200 MHz.
EXTERNAL GATE INPUT	<+0.3V to gate output on. >+1.3V to gate output off. Maximum input level is +5.0V. 50 ohm input impedance. Synchronous gate input assures that only complete output pulses are generated.
TRIGGER AND CLOCK OUTPUTS	Trigger - positive edge at time T0. Clock approx. 12 nS earlier. Signal amplitude is approx. +1.0V into 50 ohms, >+2.0V into high impedance.
JITTER	<0.1% of setting + 25 pSec. Applies to period, delay, and width.
WAVEFORM DISTORTION	± 5% or + 175 mV, whichever is greater for 5 volt plug in. ±5% or + 350 mV, whichever is greater for 10 volt plug in.
RAMP LINEARITY	±5% for transitions > 10 nSec
DOUBLE PULSE PERIOD	>10 nSec.
DOUBLE PULSE SPACING	>5 nSec. or 2X programmed width, whichever is greater.

PROGRAMMING ACCURACY		Settings	Spec.
	Period	All	± 1% of setting
	Delay,width*	<26 uS	±2% + 1 nS of setting
	(Range extender option)	>26 uS	±5% + 1 nS of setting
	*(See Section 3.1 - Width)		
	Rise & fall	All	±2% + 1 nS of setting
	VHi, VLo (Full Scale)	5V plug in 10V plug in	±2% +25 mV ±2% +50 mV

RESOLUTION .1% of full scale or <1% of setting.

REPEATABILITY <.1% of setting

SETTLING TIME <2.5 mSec. for attenuation and polarity.

IEEE-488 INTERFACE Subsets: SH1, AH1, T6, L4, SR1, RL1, PP2, DC1, DT1 and CO.

RS-232 INTERFACE Baud Rates: 110, 300, 1200, 2400, 4800, 9600, and 19200
Parity: Odd, Even, or None
Data Bits: 5, 6, 7, or 8
Stop Bits: 1, 1.5, or 2

SIGNAL CONNECTORS Pulse output: SMA
All others: BNC
(except remote interface)

POWER REQUIREMENTS	Voltage: 100, 117, 217, or 234 V AC (10%) Frequency: 50 to 60 Hz. Wattage (117 V): 500 VA
HEIGHT	8.75 in; 22.3 cm
WIDTH	19.00 in; 48.2 cm
DEPTH	Rack mounting depth: 23.00 in; 58.4 cm Overall depth: 25.00 in; 63.5 cm
WEIGHT	Chassis with front panel and no outputs: 75 lbs.; 34 kg. Output chan.: 3.5 lbs.; 1.6 kg.
SHIPPING WEIGHT	4 channel unit with front panel: 110 lbs.; 50 kg.
MODEL NUMBERS	SPG2000 -- Mainframe with CRT and keyboard.
	SPG2001 -- Mainframe without front panel.
	P2005 -- 5V output channel.
	P2005E -- 5V extended range.
	P2010 -- 10V output channel.
	P2010E -- 10V extended range.
	C2100 -- Ext. channel drive clock board option.

SPG2000 SERIES VERIFICATION PROCEDURE

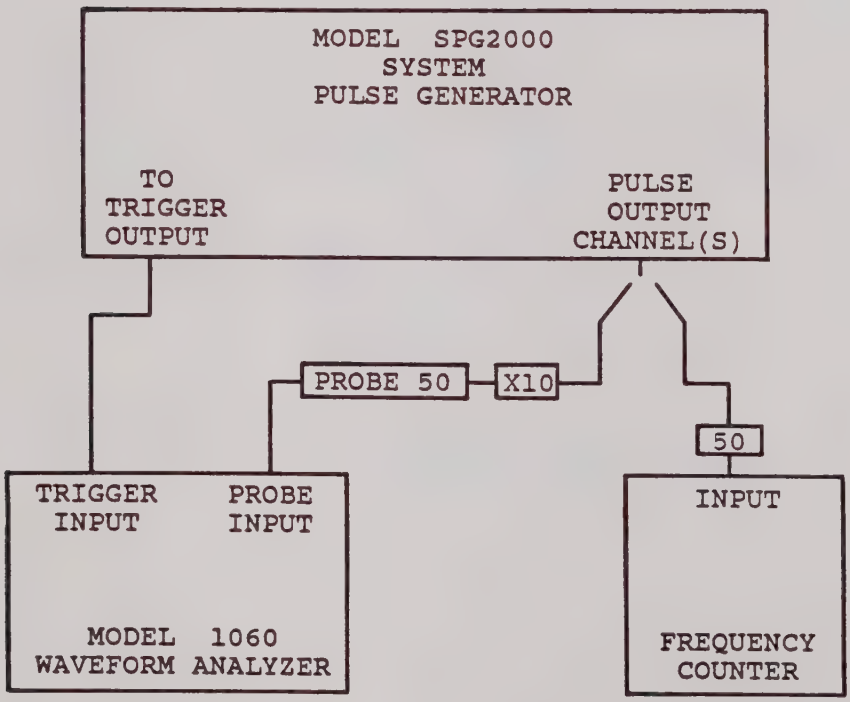
PERFORMANCE CHECK PROCEDURE

The following procedures check functional capability and parameter accuracy. The procedure can be used for incoming inspection or for periodic performance checks that are a part of scheduled maintenance.

TEST EQUIPMENT REQUIRED:

1 GHz bandpass oscilloscope, 350 pS risetime minimum. The EH model 1060 waveform analyzer with an EH 961 probe meets these specifications. Use a X10 attenuator between the SPG2000 output and the probe.

Frequency counter, 200 MHz minimum.



TEST EQUIPMENT SETUP

Figure 1-1

FUNCTIONAL CHECK

1. Connect the SPG2000 and 1060 as shown in Figure 1-1. ALL OUTPUTS OF THE SPG2000 SHOULD BE TERMINATED IN 50.

2 Turn both units on and allow the 1060 to warmup for a few minutes. The SPG2000 does not need a warmup period but none of the outputs are active until it has completed its selftest routine.

3. When the SPG2000 is shipped from the factory each channel has been set to a standard turn-on program setting. Verify the settings on the unit with the listing below. To change the settings position the cursor over the value you wish to change, enter the new values and depress one of the terminator keys.
Example: to set the period to 100 nanoseconds (nS) depress the "1","0","0", and "NANO" keys.

STANDARD FACTORY-SET TURN-ON PROGRAM

External CLK Trigger...OFF	Channel Clock EXT triggers...OFF
Burst .....OFF	Internal Period.....100 nS
Delay ..... 10.00 nS	Width ..... 10.00 nS
Lead ..... 2.000 nS	Trail ..... 2.000 nS
Vhi ..... 650.0 mV	Vlow ..... 650.0 mV
Inv ..... OFF	Dbl ..... OFF
Protection Level..... 1	Setup 00

4. Adjust the oscilloscope to display a full cycle of the waveform. Change Vhi to 5.000 volts on CH 1.

5. Measure the pulse period. Spec. ± 1%.
The period should be 100 nS within ± 1 nS.

6. Measure the pulse width. Spec. ± 2% + 1 nS.
The pulse width should be 10 nS within ± 1.2 nS

7. Measure the leading and trailing edges. Spec.±2% + 1nS.
Both edges should measure 2nS within ± 1.04 nS

8. Measure the amplitude (Vhi-Vlow).
Spec. 5 volt channel ± 2% + 25 mV. Measure 5 V ± 125 mV
10 volt channel ± 2% + 50 mV. Measure 5 V ± 150 mV

9. Measure the delay. Spec. ± 2% + 1 nS. Align the leading edge of the pulse with one of the graticule lines on the oscilloscope. The timebase should be set to 5 nS/Div. Change the Delay setting to 20 nS. Change in delay should measure 20 nS ± 1.4 nS.

10. Repeat steps 4 through 9 for each additional channel.

11. Refer to Model C2100 Clock Board Verification Procedure to verify operation of external trigger inputs.

SPG2000 SERIES PERFORMANCE CHECK

1. INITIAL SETUP

All outputs of the SPG2000 should be terminated in 50 .
Modify the settings of the SPG2000 to the following:

External CLK Trigger ...OFF	Channel Clock EXT Triggers...OFF
Burst .....OFF	Internal Period ..... 5.000 nS

EACH CHANNEL

Delay ..... 2.000 nS	Width ..... 2.000 nS
Lead ..... 900.0 pS	Trail ..... 900.0 pS
Vhi ..... 5.000 V	Vlow ..... 0.000 V
Inv ..... OFF	Dbl ..... OFF
Protection Level 1	Setup 00

2. CLOCK CHECK

a. Connect the SPG2000 and the frequency counter as shown in Figure 1-1 and apply power.

b. Measure the pulse period. Spec. ± 1%.
The period should be 5 nS ± 50 pS.

c. Following the table below, change the period of pulse generator to the value in the left column and check the output of channel 1 to the spec given.

PULSE GENERATOR SETTING	FREQUENCY COUNTER READING MIN	MAX
10nS	9.0 nS	11.0 nS
50 nS	49.5 nS	50.5 nS
100 nS	99 nS	101 nS
500 nS	495 nS	505 nS
1 uS	990 nS	1.01 uS
50 uS	49.5 uS	50.5 uS
100 uS	99 uS	101 uS
500 uS	495 uS	505 uS
1 mS	990 mS	1.01 mS
50 mS	49.5 mS	50.5 mS
100 mS	99 mS	101 mS
500 mS	495 mS	505 mS
1 S	990 mS	1.01

d. Modify the SPG2000 settings as follows:

Internal Period . . . . . 10.00 nS
Burst . . . . . ON
Count 00010

e. Move the cursor to the right of "Start?". To initiate a burst depress the "ENTER" key. Verify with the counter that the SPG2000 puts out a burst of 10 pulses.

f. Change the burst count to various numbers between 1 and 65535 and verify the output.

g. Modify the SPG2000 settings as follows:

Burst . . . . . OFF

Refer to Model C2100 Clock Board Verification Procedure to verify operation of independent external trigger inputs.

3. WIDTH CHECK

a. Modify the settings of the SPG2000 to those given in section #1 Initial Setup of the Calibration Check.

b. Modify the SPG2000 settings as follows:

Internal Period 500.0nS

c. Use the 1060/oscilloscope to measure the pulse width. Spec.± 2% + 1 nS. (<26 uS). The pulse width should be 2 nS ± 1.04 nS.

d. Using the following table check the width settings listed below.

WIDTH SETTING	MEASURED VALUE MIN	MAX
15 nS	13.7 nS	16.3 nS
30 nS	28.4 nS	31.6 nS
120 nS	116.6 nS	123.4 nS
150 nS	146 nS	154 nS
200 nS	195 nS	205 nS

e. Modify the SPG2000 settings as follows:

Internal Period . . . . . 100.0 uS

f. Continue the width calibration check.

WIDTH SETTING	MEASURED VALUE MIN	MAX
2 uS	1.96 uS	2.06 uS
5 uS	4.90 uS	5.10 uS
25 uS	24.5 uS	25.5 uS

g. If the SPG 2000 is not equipped with the extended range option skip to section #4 Delay Check. If unsure as to option try to enter 50 uS. If the unit responds by changing the width the option is present.

h. Modify the SPG2000 settings to the following to check the extended range calibration:

Internal Period . . . . . 1.000 mS

i. Continue the width calibration check.
Spec. ± 5% + 1 nS. (<26 uS)

WIDTH SETTINGS	MEASURED VALUE MIN	MAX
50 uS	47.5 uS	52.5 uS
300 uS	285 uS	315 uS

j. Modify the SPG2000 settings as follows:

Internal Period . . . . . 1.000 S

k. Continue the width calibration check.

WIDTH SETTINGS	MEASURED VALUE MIN	MAX
4 mS	3.02 mS	4.08 mS
10 mS	9.50 mS	10.5 mS
80 mS	76 mS	84 mS
100 mS	95 mS	105 mS
500 mS	475 mS	525 mS
900 mS	855 mS	945 mS

l. Width calibration check complete.

4. DELAY CHECK

There are two versions of the SPG2000 clock board.

SPG2000's with the C2100 External Channel Trigger option have minimum delay in protection level 1 of 2 nS ± 1 nS with respect to T0. The delay to the first pulse in the double pulse mode is 0 nS ± 1 nS. Follow the calibration check as written.

SPG2000's without the C2100 option have a mimimum programmable delay of 2 nS in protection level 1. The minimum delay is 11.5 nS ±2 nS with respect to T0 and the delay to the first pulse in the double pulse mode is 9.5 nS ±2 nS. This applies to channel #1 only. When following the procedure remember to add this factor when considering the measurements.

a. Modify the settings of the SPG2000 to those given in Section #1 Initial Setup of the Calibration Check.

b. Modify the SPG2000 settings as follows:

Internal Period . . . . 500.0 nS

c. Use the 1060/oscilloscope to measure the delay from T0 to the 50% point of the leading edge of the pulse. Spec.± 5% +1 nS. The delay should be 2 nS ±1.02 nS.

d. Using the following table check the delay settings listed below.

DELAY SETTING	MEASURED VALUE MIN	MAX
15 nS	13.7 nS	16.3 nS
30 nS	28.4 nS	31.5 nS
120 nS	116.6 nS	123.4 nS
150 nS	146 nS	154 nS
200 nS	195 nS	205 nS

e. Modify the SPG2000 settings as follows:

Internal Period . . . . 100.0 uS
Width . . . . . 100.0 nS

f. Continue the delay calibration check.

DELAY SETTING	MEASURED VALUE MIN	MAX
2 uS	1.96 uS	2.06 uS
5 uS	4.90 uS	5.10 uS
25 uS	24.5 uS	25.5 uS

g. If the SPG2000 is not equiped with the extended range option skip to Section #5 Delay Check. If unsure as to option try to enter 50 uS. If the unit responds by changing the delay the option is present.

h. Modify the SPG2000 settings to the following to check the extended range calibration:

Internal Period . . . . . 1.000 mS

i. Continue the delay calibration check.
Spec. ± 5% + 1 nS.

DELAY SETTING	MEASURED VALUE MIN	MAX
50 uS	47.5 uS	52.5 uS
300 uS	285 uS	315 uS

j. Modify the SPG2000 settings as follows:

Internal Period . . . . . 1.000 S

k. Continue the delay calibration check.

DELAY SETTING	MEASURED VALUE MIN	MAX
4 mS	3.02 mS	4.08 mS
10 mS	9.50 mS	10.5 mS
80 mS	76 mS	84 mS
100 mS	95 mS	105 mS
500 mS	475 mS	525 mS
900 mS	855 mS	945 mS

l. Delay calibration check complete.

5. LEADING/TRAILING EDGE CHECK

a. Modify the settings of the SPG2000 to those given in Section #1 Initial Setup of the Calibration Check.

b. Modify the SPG2000 settings as follows:

Internal Period . . . . . 100.0 nS
Delay . . . . . 5.000 nS
Width . . . . . 50.00 nS
Lead/Trail . . . . . 0.876 pS

c. The minimum edge speed for the 5 volt and 10 volt channels is different.
Spec. 5 V channel --- < 1 nS ± 2% + 1 nS.
10 V channel --- < 2 nS ± 2% + 1 nS.
A 10 V channel should meet the spec at 10 V.

d. Use the 1060/oscilloscope to measure the edges. All measurements are 10% to 90%.

5 V channel --- < 1 nS
10 V channel --- < 2 nS

e. Using the following table check the leading and trailing edge settings listed below.

LEAD/TRAIL SETTING	MEASURED VALUE MIN	MAX
12 nS	10.76 nS	13.26 nS
15 nS	13.7 nS	16.3 Ns

f. Modify the SPG2000 settings as follows:

Internal Period . . . . . 10.00 uS
Delay . . . . . 300.0 nS
Width . . . . . 600.0 nS

g. Continue the lead/trail calibration check.

LEAD/TRAIL SETTINGS	MEASURED VALUE MIN	MAX
100 nS	97 nS	100 nS
200 nS	195 nS	205 nS
250 nS	244 nS	256 nS

h. Modify the SPG2000 settings as follows:

Internal Period . . . . . 50.00 uS
Delay . . . . . 7.500 uS
Width . . . . . 12.50 Us

i. Continue the lead/trail calibration check.

LEAD/TRAIL SETTINGS	MEASURED VALUE MIN	MAX
1 uS	980 nS	1.02 uS
2 uS	1.96 uS	2.04 uS

j. The leading/trailing edge calibration check is complete.

6. AMPLITUDE CHECK

a. Modify the settings of the SPG2000 to those given in Section #1 Initial Setup of the Calibration Check.

b. Modify the SPG2000 settings as follows:

Internal Period . . . . . 10.00 uS
Width . . . . . 50.00 nS

c. Use the 1060/oscilloscope to measure the amplitude of the pulse.
Spec. 5 V channel --- ± 2% + 25 mV.
10 V channel --- ± 2% + 50 mV.
The amplitude should measure as follows:
5 V channel --- 5 V ± 125 mV.
10 V channel --- 5 V ± 150 mV.

d. Using the following table check the amplitude settings given below.

Vhi SETTING (Vlow = 0 V)	MEASURED VALUE 5 V CHAN MIN	5 V CHAN MAX	10 V CHAN MIN	10 V CHAN MAX
10 V	N/A	N/A	9.75 V	10.25 V
2.5 V	2.425 V	2.575 V	2.4 V	2.6 V
2.0 V	1.935 V	2.065 V	1.91 V	2.09 V
1.25 V	1.2 V	1.3 V	1.175 V	1.325 V
750 mV	710 mV	790 mV	685 mV	815 mV
625 mV	587 mV	658 mV	537 mV	688 mV
500 mV	465 mV	535 mV	N/A	N/A
312 mV	281 mV	343 mV	N/A	N/A

e. The amplitude check is complete.

7. DOUBLE PULSE SPACING CHECK

a. Modify the settings of the SPG2000 to those given in Section !3 Initial Setup of the Calibration Check.

b. Modify the SPG2000 settings as follows:

Internal Period . . . . . 10.00 nS
Delay . . . . . 5.000 nS
Width . . . . . 2.000 nS
Dbl . . . . . ON

c. Use the 1060/oscilloscope to display the pulses. Verify the presence of two complete pulses.
Spec. Minimum double pulse spacing --- 5 nS or 2 X the programmed width whichever is greater. It may be necessary to reduce delay.

d. The double pulse spacing check is complete.

APPENDIX G

MODEL C2100 CLOCK VERIFICATION PROCEDURE

INDEPENDENT EXTERNAL CHANNEL TRIGGER

VERIFICATION PROCEDURE

TEST EQUIPMENT REQUIRED:

Pulse Generator: EH 136A, 137A or equivalent.

Generator must be capable of producing ECL and TTL levels with a 50% duty cycle at a pulse repetition rate of 50 MHz or greater.

Oscilloscope: 50 MHz bandwidth minimum

Note: A 1 GHz bandwith oscilloscope such as the EH 1060 is necessary to check full performance capabilities of the SPG2000. This verification procedure is intended only to check the basic operation of the independent external channel trigger and external clock trigger inputs.

Miscellaneous: Cables, adaptors, and loads.

Pulse channel outputs are SMA connectors. External trigger inputs and T0 trigger output are BNC connectors. All signals except T0 require 50 ohm loads.

WARNING: EXTERNAL DRIVE INPUTS FOR CHANEL 1 THROUGH CHANNEL 4 (J114 THROUGH J117) SHOULD BE ECL LEVELS.

ALL OTHER BNC INPUTS REQUIRE TTL LEVELS.

C2100 CLOCK BOARD VERIFICATION PROCEDURE

A. PRELIMINARY PROCEDURE

CAUTION: Care should be taken to insure that each pulse channel output is terminated with a 50 ohm load at any time AC power is present. Apply power to the test equipment and allow it to warm up. No warmup time is required by the SPG2000 but signals will not be present at the outputs until completion of the selftest procedure.

B. CLOCK AND T0 OPERATIONAL CHECK

1. Using the oscilloscope verify the internal clock output at J109 (CLOCK) and the T0 output at J108 are functional at the levels specified below.

   J109 CLOCK output .. 50% duty cycle.
   > +1.5 V into 50 ohms.
   > +3.0 V into high-z.

   J108 T0 output ..... Positive edge at time T0.
   1-4 nS width, freq. dep.
   > +1.5 V into 50 ohms.
   > +3.0 V into high-z.

C. INTERNAL CLOCK OPERATIONAL CHECK

1. Program the SPG2000 to the following settings:

   External channel trigger(s)..... OFF
   The indicators for this function are located below the EXT in the upper left-hand corner of the display
   External CLK Trigger ..... OFF
   Internal Period ..... 50 nS
   Burst ..... OFF
   Delay ..... 10 nS
   Width ..... 25 nS
   Lead and Trail ..... 2 nS
   Vhi ..... 5 V
   Vlow ..... 0 V
   Inv and Dbl ..... OFF

   Set each channel to the same delay, width, etc.

2. Using the oscilloscope verify the operation of each pulse channel output -- connectors J101 through J104.

D. EXTERNAL CLOCK OPERATIONAL CHECK

1. Modify the SPG2000 settings to the following:

   External CLK Trigger ..... ON

2. Using the oscilloscope adjust the EH 136A to produce positive pulse into 50 ohms with the following characteristics:

   Baseline .... 0 V Pulse top ..... 1.5 V
   Period ..... 50 nS Width .. 5 nS to 25 nS
   Delay ..... Min. Lead/Trail ..... Min.

3. Connect the output of the EH 136A to J113 on the rear panel of the SPG2000. This is the CLOCK EXTERNAL DRIVE input.

4. Using the oscilloscope verify that channel 1 of the SPG2000 is producing a pulse output. It is unnecessary to check the other outputs.

E. EXTERNAL CHANNEL TRIGGER OPERATIONAL CHECK

1. Modify the SPG2000 to the following:

   External channel trigger(s) ..... ON
   External CLK Trigger ..... OFF or ON

2. Using the oscilloscope adjust the EH 136A to produce a positive pulse into 50 ohms with the following characteristics:

   Baseline .... -1.3 V Pulse top ... -0.3 V
   Period ..... 50 nS Width ..... 25 nS
   Delay ..... Min. Lead/Trail ..... Min.

3. Connect the EH 136A to J114 CHAN. 1 EXTERNAL DRIVE.

4. Using the oscilloscope verify the operation of pulse output channel 1 at J101 CHAN. 1 OUTPUT.

5. Repeat steps 3 and 4 to verify any additional channels using the table below.

EXTERNAL DRIVE INPUT	PULSE OUTPUT CHANNEL
J115 CHAN. 2	CHAN. 2 OUTPUT
J116 CHAN. 3	CHAN. 3 OUTPUT
J117 CHAN. 4	CHAN. 4 OUTPUT

This completes the C2100 verification procedure.

SPG2000 SERIES DAC RANGES

Period

Full Range -- 5nS to 10nS

Other settings by divider.

Delay & Width

All Boards -- Range	0	2	nS to	15.99	nS
	1	16	nS to	127.9	nS
	2	128	nS to	2.047	uS
	3	2.048	uS to	32.767	uS
Extended Ranges	4	33	uS to	349.9	uS
	5	350	uS to	4.999	mS
	6	5	mS to	84.99	mS
	7	85	mS to	1	S

Leading & Trailing Edge

5V Board -- Range	0	875	pS to	13.99	nS
	1	14	nS to	219.9	uS
	2	220	us to	5	uS
10V Board -- Range	0	1.6	nS to	17.99	nS
	1	18	nS to	399.9	uS
	2	400	uS to	5	uS

Amplitude

5V Board --	5 V	to	2.5 V	(DAC range)
	2.5 V	to	312 mV	(attenuator ranges) (x2, x4, x8)
10V Board --	10 V	to	5 V	(DAC range)
	5 V	to	625 mV	(attenuator ranges) (x2, x4, x8)

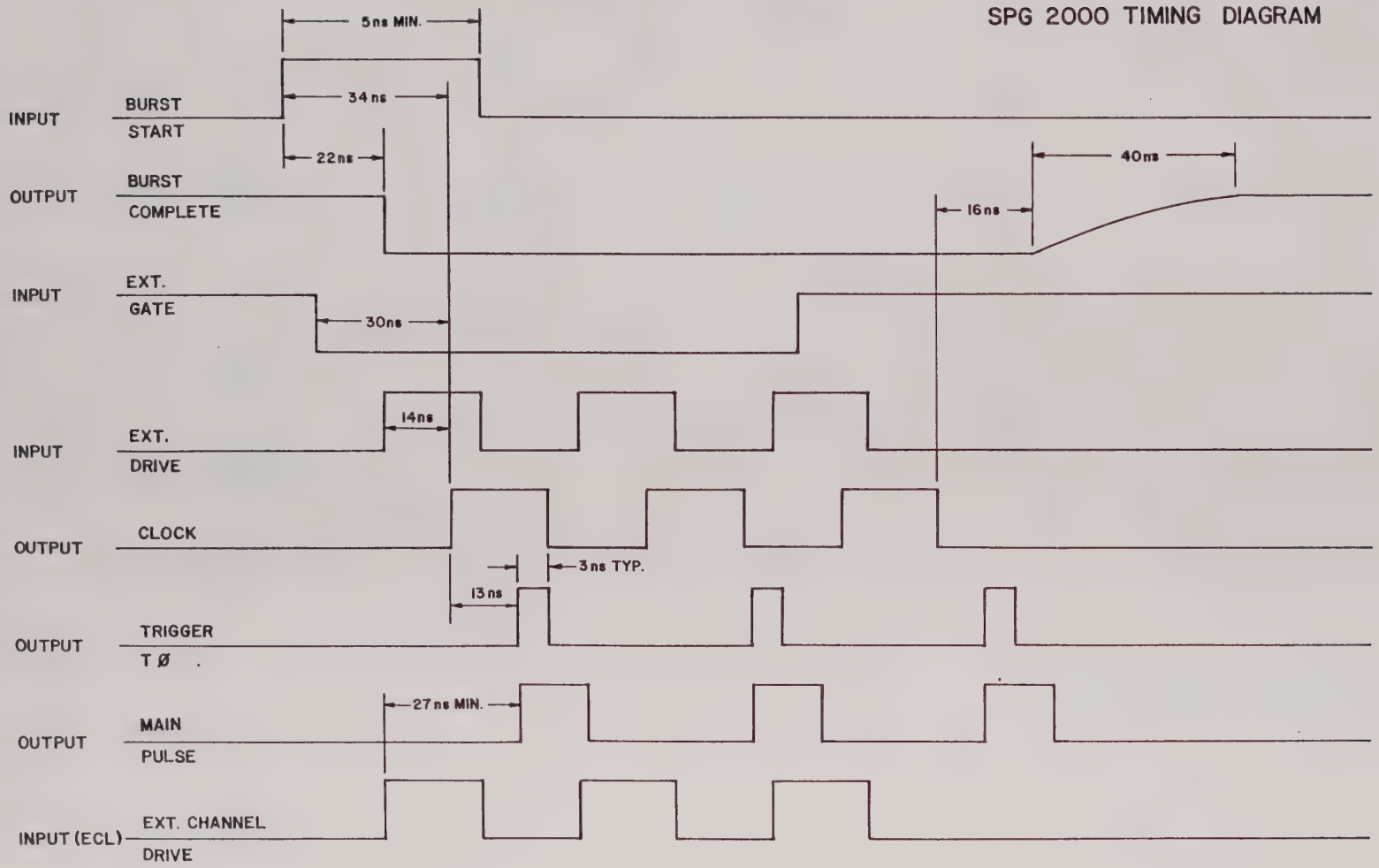
Burst

Count -- 1 to 65535

APPENDIX I

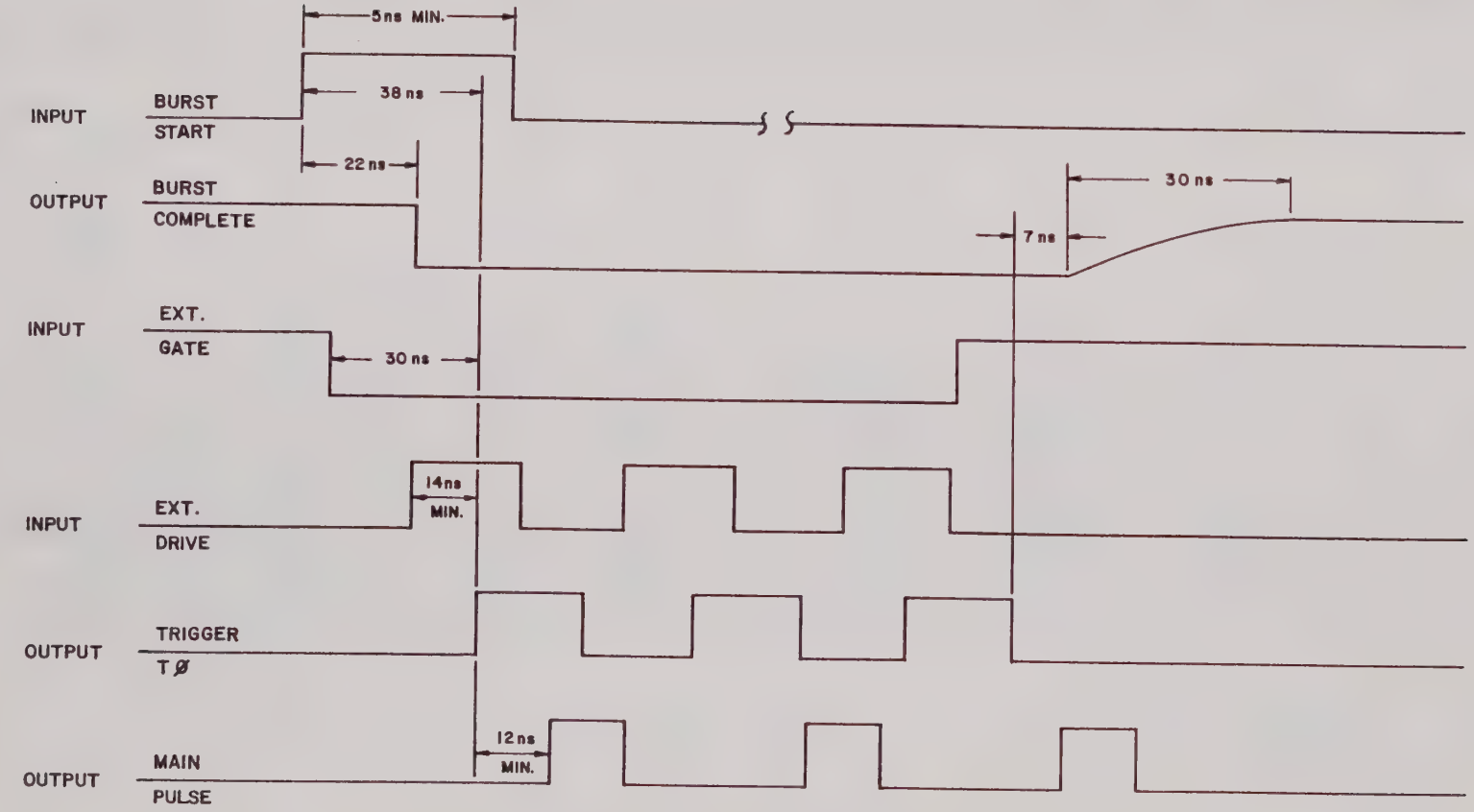
C 2100 CLOCK BOARD

SPG 2000 TIMING DIAGRAM



STANDARD CLOCK BOARD

SPG 2000 TIMING DIAGRAM



MODEL SPG2000

SECTION 5

NOTES AND CHANGES

SECTION 5 NOTES

5.1 VHi - VLo RANGES

The unattenuated output voltage swing (Vs = VHi - VLo) range of the SPG2000 series pulse generator is 2.5V to 5V for a 5V channel and is 5V to 10V for a 10V channel.

Smaller voltage swings are achieved by using attenuators in the x2, x4, and x8 ranges.

There are limitations on the minimum Vs settings using this method: (See Figures 5-1 and 5-2)

MINIMUM VOLTAGE SWINGS

	5 VOLT CHANNEL	10 VOLT CHANNEL
Vs ≥	313 mV (1)	625 mV (2)
Vs ≥	625 mV (2)	1.25 V (3)
Vs ≥	1.25 V (3)	2.5 V (4)
Vs ≥	2.5 V (4)	5.0 V (5)
Vs ≥	5.0 V (6)	10.0 V (6)

(1) If Vlow offset = 0 ± 0.625 V
(2) If Vlow offset = 0 ± 1.25 V
(3) If Vlow offset = 0 ± 2.5 V
(4) If Vlow offset = 0 + 7.5 V, - 5 V
(5) If Vlow offset = 0 + 10 V, - 5 V
(6) For any offset.

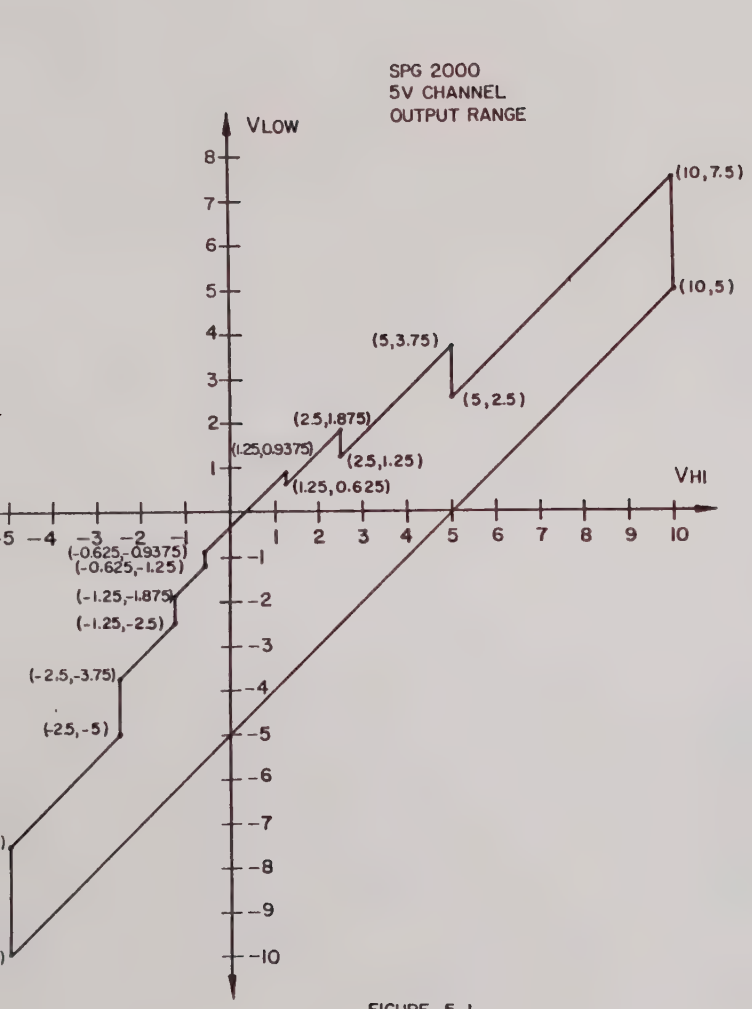


FIGURE 5-1

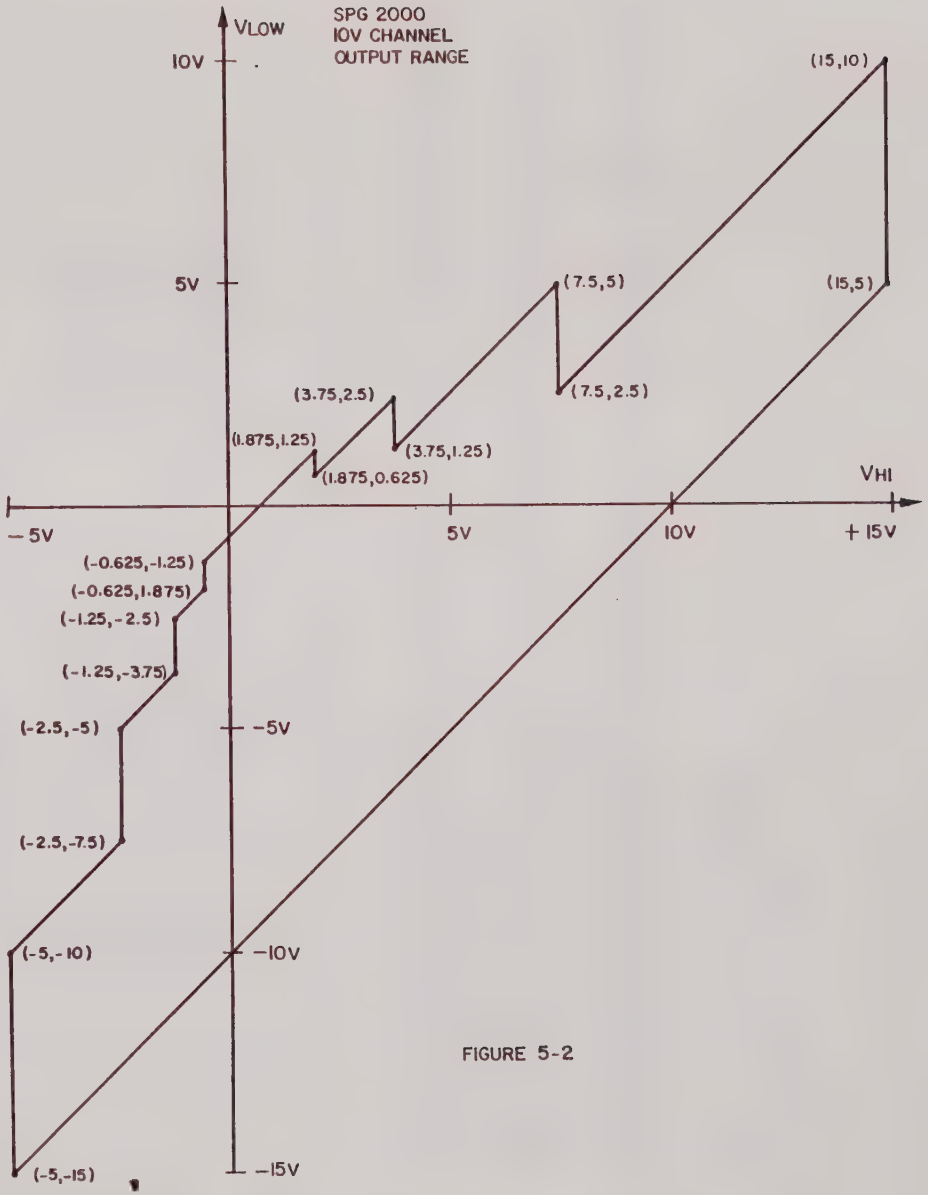


FIGURE 5-2

MP MASTER
MA35748